

K.S.INSTITUTE OF TECHNOLOGY, BANGALORE
(*AFFILIATED TO VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELGAUM*)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGG.

ENGINEERING MATHEMATICS-IV

(Common to all Branches)

Course Title: Engineering Mathematics-IV
15MAT41Credits:04
Contact Hours/Week: 04
Exam. Marks:80
Exam. Hours: 03

Course Code:
L-T-P:4-0-0
Total Hours:50
IA Marks:20

Modules	RBT Level
Module-1	
Numerical Methods : Numerical solution of ordinary differential equations of first order and first degree, Taylor's series method, modified Euler's method, Runge - Kutta method of fourth order. Milne's and Adams- Bashforth predictor and corrector methods (No derivations of formulae).	L1, L3
Module-2	
Numerical Methods: Numerical solution of second order ordinary differential equations, Runge-Kutta method and Milne's method. Special Functions: Series solution-Frobenius method. Series solution of Bessel's differential equation leading to $J_n(x)$ -Bessel's function of first kind. Basic properties and orthogonality. Series solution of Legendre's differential equation leading to $P_n(x)$ -Legendre polynomials. Rodrigue's formula, problems.	L3
Module-3	
Complex Variables: Review of a function of a complex variable, limits, continuity, differentiability. Analytic functions-Cauchy-Riemann equations in cartesian and polar forms. Properties and construction of analytic functions. Complex line integrals-Cauchy's theorem and Cauchy's integral formula, Residue, poles, Cauchy's Residue theorem (without proof) and problems. Transformations: Conformal transformations, discussion of transformations: $w = z^2$, $w = e^z$, $w = z + 1$, $z = z + i0$ and bilinear transformations- problems.	L1, L3, L3
Module-4	
Probability Distributions: Random variables (discrete and continuous), probability mass/density functions. Binomial distribution, Poisson distribution. Exponential and normal distributions, problems.	L3

2. E. Kreyszig: <i>Advanced Engineering Mathematics</i> , John Wiley & Sons, 10 th Ed., 2015.	
<p>Reference Books:</p> <ol style="list-style-type: none"> 1. N.P.Bali and Manish Goyal: <i>A Text Book of Engineering Mathematics</i>, Laxmi Publishers, 7th Ed., 2010. 2. B.V.Ramana: <i>"Higher Engineering Mathematics"</i> Tata McGraw-Hill, 2006. 3. H. K. Dass and Er. Rajnish Verma: <i>"Higher Engineering Mathematics"</i>, S. Chand publishing, 1st edition, 2011. 	
<p>Web Link and Video Lectures:</p> <ol style="list-style-type: none"> 1. http://nptel.ac.in/courses.php?disciplineID=111 2. http://www.khanacademy.org/ 3. http://www.class-central.com/subject/math 	

ADDITIONAL MATHEMATICS - II
B.E., IV Semester, Common to all Branches
(A Bridge course for Lateral Entry students of IV Sem. B. E.)
[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15MATDIP41	IA Marks	--
Number of Lecture Hours/Week	03	Exam marks	80
Total Number of Lecture Hours	40 (08 Hours per Module)		
Credits – 00			
Course Objectives: This course will enable students to:			
<ul style="list-style-type: none"> • Understand essential concepts of linear algebra. • Solve second and higher order differential equations. • Understand Laplace and inverse Laplace transforms and elementary probability theory. 			
Modules			RBT Level
Module-1			
Linear Algebra: Introduction-rank of matrix by elementary row operations - Echelon form. Consistency of system of linear equations - Gauss elimination method. Eigen values and Eigenvectors of a square matrix. Application of Cayley-Hamilton theorem (without proof) to compute the inverse of a matrix- Examples.			L1,L3
Module-2			
Higher order ODE's: Linear differential equations of second and higher order equations with constant coefficients. Homogeneous /non- homogeneous equations. Inverse differential operators. Solutions of initial value problems. Method of undetermined coefficients and variation of parameters.			L1,L3
Module-3			
Laplace transforms: Laplace transforms of elementary functions. Transforms of derivatives and integrals, transforms of periodic function and unit step function-Problems only.			L1,L2
Module-4			
Inverse Laplace transforms : Definition of inverse Laplace transforms. Evaluation of Inverse transforms by standard methods. Application to solutions of Linear differential equations and simultaneous differential equations.			L1,L2
Module-5			
Probability: Introduction. Sample space and events. Axioms of probability. Addition and multiplication theorems. Conditional probability – illustrative examples. Bayes' theorem-examples.			L1,L2
Course Outcomes: On completion of this course, students are able to:			
<ul style="list-style-type: none"> • Solves systems of linear equations in the different areas of linear algebra. • Solves second and higher order differential equations occurring in electrical circuits, damped/un-damped vibrations. 			

<ul style="list-style-type: none"> • Describe Laplace transforms of standard and periodic functions. • Determine the general/complete solution to linear ODE using inverse Laplace transforms. • Recall basic concepts of elementary probability theory and, solve problems related to the decision theory, synthesis and optimization of digital circuits. 	
<p>Question paper pattern:</p> <ul style="list-style-type: none"> • The question paper will have ten questions. • Each full Question consisting of 16 marks • There will be 2 full questions (with a maximum of four sub questions) from each module. • Each full question will have sub questions covering all the topics under a module. • The students will have to answer 5 full questions, selecting one full question from each module. 	
<p>Text Book :</p> <p><i>B.S. Grewal: Higher Engineering Mathematics, Khanna Publishers, 43rd Ed., 2015.</i></p>	
<p>Reference Books:</p> <ol style="list-style-type: none"> 1. <i>E. Kreyszig: Advanced Engineering Mathematics, John Wiley & Sons, 10th Ed., 2015.</i> 2. <i>N.P. Bali and Manish Goyal: A Text Book of Engineering Mathematics, Laxmi Publishers, 7th Ed., 2007.</i> 	

<u>MICROPROCESSORS</u> [As per Choice Based Credit System (CBCS) scheme] SEMESTER – IV (EC/TC)			
Subject Code	15EC42	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of Lecture Hours	50 (10 Hours per Module)	Exam Hours	03
CREDITS – 04			
Course objectives: This course will enable students to: <ul style="list-style-type: none"> • Familiarize basic architecture of 8086 microprocessor • Program 8086 Microprocessor using Assembly Level Language • Use Macros and Procedures in 8086 Programs • Understand interfacing of 16 bit microprocessor with memory and peripheral chips involving system design • Understand the architecture of 8088, 8087 Coprocessor and other CPU architectures 			
Modules			RBT Level
Module -1			
8086 PROCESSOR: Historical background (refer Reference Book 1), 8086 CPU Architecture (1.1 – 1.3 of Text). Addressing modes, Machine language instruction formats, Machine coding the program (2.2, 2.1, 3.2 of Text). INSTRUCTION SET OF 8086: Data transfer and arithmetic instructions. Control/Branch Instructions, Illustration of these instructions with example programs (2.3 of Text).			L1, L2, L3
Module -2			
Logical Instructions, String manipulation instructions, Flag manipulation and Processor control instructions, Illustration of these instructions with example programs. Assembler Directives and Operators, Assembly Language Programming and example programs (2.3, 2.4, 3.4 of Text).			L1, L2, L3
Module -3			
Stack and Interrupts: Introduction to stack, Stack structure of 8086, Programming for Stack. Interrupts and Interrupt Service routines, Interrupt cycle of 8086, NMI, INTR, Interrupt programming, Passing parameter to procedures, Macros, Timing and Delays. (Chap. 4 of Text).			L1, L2, L3
Module -4			

<p>8086 Bus Configuration and Timings: Physical memory Organization, General Bus operation cycle, I/O addressing capability, Special processor activities, Minimum mode 8086 system and Timing diagrams, Maximum Mode 8086 system and Timing diagrams. (1.4 to 1.9 of Text).</p> <p>Basic Peripherals and their Interfacing with 8086 (Part 1) : Static RAM Interfacing with 8086 (5.1.1), Interfacing I/O ports, PIO 8255, Modes of operation – Mode-0 and BSR Mode, Interfacing Keyboard and 7-Segment digits using 8255 (Refer 5.3, 5.4, 5.5 of Text).</p>	<p>L1, L2, L3</p>
<p>Module 5</p>	
<p>Basic Peripherals and their Interfacing with 8086 (Part 2): Interfacing ADC-0808/0809, DAC-0800, Stepper Motor using 8255 (5.6.1, 5.7.2, 5.8). Timer 8254 – Mode 0, 1, 2 & 3 and Interfacing programmes for these modes (refer 6.1 of Text).</p> <p>INT 21H DOS Function calls - for handling Keyboard and Display (refer Appendix-B of Text).</p> <p>Other Architectures: Architecture of 8088 (refer 1.10 upto 1.10.1 of Text) and Architecture of NDP 8087 (refer 8.3.1, 8.3.5 of Text).</p> <p>Von-Neumann & Harvard CPU architecture and CISC & RISC CPU architecture (refer Reference Book 1).</p>	<p>L1, L2, L3</p>
<p>Course Outcomes: At the end of the course students will be able to:</p> <ul style="list-style-type: none"> • Identify the different CPU architectures, 8086 Microprocessor architecture and addressing modes of 8086. • Make use of the instruction set and addressing modes of 8086 to develop assembly language programs • Make use of stacks , interrupts to develop programs • Model the static memory chips, 8255 & 8254, and use of INT 21 DOS interrupt function calls to handle keyboard and display • Experiment with 8086 Microprocessor the ADC-0808, DAC-0800 and stepper motors using PPI 8255 with 8086. 	
<p>Question paper pattern:</p> <ul style="list-style-type: none"> • The question paper will have ten questions. • Each full Question consisting of 16 marks • There will be 2 full questions (with a maximum of Three subquestions) from each module. • Each full question will have subquestions covering all the topics under a module. • The students will have to answer 5 full questions, selecting one full question from each module. 	

Reference Books:

1. Microprocessor and Interfacing - Douglas V Hall, SSSP Rao, 3rd edition TMH, 2012.
2. Microcomputer systems-The 8086 /8088 Family –Y.C. Liu and A. Gibson, 2nd edition, PHI-2003.
3. The 8086Microprocessor: Programming &InterfacingthePC – Kenneth J Ayala, CENGAGE Learning, 2011.
4. The Intel Microprocessor, Architecture, Programming and Interfacing -BarryB.Brey, 6e, Pearson Education/PHI, 2003.

TextBook:

Advanced Microprocessors and Peripherals - A.K. Ray and K.M. Bhurchandi, TMH, 3rd Edition, 2012, ISBN 978-1-25-900613-5.

Web Link and Video Lectures:

1. <https://www.coursera.org/courses?query=microprocessor>
2. <https://www.udemy.com/course/certificate-program-in-introduction-to-microprocessors/>

<u>CONTROL SYSTEMS</u> [As per Choice Based Credit System (CBCS) scheme] SEMESTER – IV (EC/TC)			
Subject Code	15EC43	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of LectureHours	50(10 Hours per Module)	Exam Hours	03
CREDITS – 04			
Course objectives: This course will enable students to: <ul style="list-style-type: none"> • Understandthebasicfeatures,configurationsandapplicationofcontrolsystems. • Understandvariousterminologiesanddefinitionsforthecontrolsystems. • Learnhowtofindamathematicalmodelofelectrical,mechanicalandelectro- mechanicalsystems. • Know how to find time response from the transferfunction. • Find the transfer function via Masons’rule. • Analyze the stability of a system from the transferfunction. 			
Modules			RBT Level
Module -1			
IntroductiontoControlSystems:TypesofControlSystems,Effectof Feedback Systems, Differential equation of Physical Systems – MechanicalSystems,ElectricalSystems,AnalogousSystems.Block diagramsandsignalflowgraphs:Transferfunctions,Blockdiagram algebra and Signal Flowgraphs.			L1, L2, L3
Module -2			
TimeResponseoffeedbackcontrolsystems:Standardtestsignals,Unit step response of First and Second order Systems. Time response specifications, Time response specifications of second order systems, steadystateerrorsanderrorconstants.IntroductiontoPI,PDandPID Controllers (excludingdesign).			L1, L2, L3
Module -3			
Stability analysis: Concepts of stability, Necessary conditions for Stability,Routhstabilitycriterion,Relativestabilityanalysis:moreon theRouthstabilitycriterion,IntroductiontoRoot-LocusTechniques, The root locus concepts, Construction of rootloci.			L1, L2, L3
Module -4			

<p>Frequency domain analysis and stability: Correlation between time and frequency response, Bode Plots, Experimental determination of transfer function. Introduction to Polar Plots, (Inverse Polar Plot excluded) Mathematical preliminaries, Nyquist Stability criterion, (Systems with transportation lag excluded) Introduction to lead, lag and lead-lag compensating networks (excluding design).</p>	<p>L1, L2, L3</p>
<p>Module -5</p>	
<p>Introduction to Digital Control System: Introduction, Spectrum Analysis of Sampling process, Signal reconstruction, Difference equations. Introduction to State variable analysis: Introduction, Concept of State, State variables & State model, State model for Linear Continuous & Discrete time systems, Diagonalisation.</p>	<p>L1, L2, L3</p>
<p>Course Outcomes: At the end of the course, the students will be able to</p> <ul style="list-style-type: none"> • Develop the mathematical model of mechanical / electrical systems and obtain its transfer function using block reduction method / Signal flow graph method • Ability to relate transient performance parameters (overshoot, rise time, peak time and settling time) for the given system and to evaluate steady state error. • Identify various stability criteria and Determine the stability of a system in the time domain using Routh-Hurwitz criterion and Root-locus technique. • Determine the stability of a system in the frequency domain using Nyquist and bode plots • Develop a control system model in continuous and discrete time using state variable techniques 	
<p>Question paper pattern:</p> <ul style="list-style-type: none"> • The question paper will have ten questions. • Each full Question consisting of 16 marks • There will be 2 full questions (with a maximum of Three subquestions) from each module. • Each full question will have subquestions covering all the topics under a module. • The students will have to answer 5 full questions, selecting one full question from each module. 	
<p>Text Book: J. Nagarath and M. Gopal, "Control Systems Engineering", New Age International (P) Limited, Publishers, Fifth edition-2005, ISBN: 81-224-2008-7.</p>	
<p>Reference Books:</p> <ol style="list-style-type: none"> 1. "Modern Control Engineering," K. Ogata, Pearson Education Asia/PHI, 4th Edition, 2002. ISBN 978-81-203-4010-7. 2. "Automatic Control Systems", Benjamin C. Kuo, John Wiley India Pvt. Ltd., 8th Edition, 2008. 3. "Feedback and Control System," Joseph J Distefano III et al., Schaum's Outlines, TMH, 2nd Edition 2007. 	

Web Link and Video Lectures:

1. <https://www.udemy.com/topic/control-systems/>
2. <https://www.coursera.org/courses?query=control%20systems>

<u>SIGNALS AND SYSTEMS</u> [As per Choice Based Credit System (CBCS) scheme] SEMESTER – IV (EC/TC)			
Subject Code	15EC44	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of Lecture Hours	50(10 Hours per Module)	Exam Hours	03
CREDITS – 04			
Course objectives: This course will enable students to: <ul style="list-style-type: none"> • Understand the mathematical description of continuous and discrete time signals and systems. • Analyze the signals in time domain using convolution difference/differential equations • Classify signals into different categories based on their properties. • Analyze Linear Time Invariant (LTI) systems in time and transform domains. • Build basics for understanding of courses such as signal processing, control system and communication. 			
Modules			RBT Level
Module -1			
Introduction and Classification of signals: Definition of signal and systems, communication and control systems as examples. Sampling of analog signals, Continuous time and discrete time signal, Classification of signals as even, odd, periodic and non-periodic, deterministic and non-deterministic, energy and power. Elementary signals/Functions: Exponential, sine, impulse, step and its properties, ramp, rectangular, triangular, signum, sinc functions. Operations on signals: Amplitude scaling, addition, multiplication, differentiation, integration (Accumulator for DT), time scaling, time shifting and time folding. Systems: Definition, Classification: linear and non-linear, time variant and invariant, causal and non-causal, static and dynamic, stable and unstable, invertible.			L1, L2, L3
Module -2			
Time domain representation of LTI System: System modeling: Input-output relation, definition of impulse response, convolution sum, convolution integral, computation of convolution integral and convolution sum using graphical method for unit step to unit step, unit step to exponential, exponential to exponential, unit step to rectangular and rectangular to rectangular only. Properties of convolution.			L1, L2, L3
Module -3			

<p>System interconnection, system properties in terms of impulse response, step response in terms of impulse response (4 Hours).</p> <p>Fourier Representation of Periodic Signals : Introduction to CTFS and DTFS, definition, properties (No derivation) and basic problems (inverse Fourier series is excluded) (06 Hours).</p>	L1, L2, L3
Module -4	
<p>Fourier Representation of aperiodic Signals: FT representation of aperiodic CT signals - FT, definition, FT of standard CT signals, Properties and their significance (4 Hours). FT representation of aperiodic discrete signals-DTFT , definition, DTFT of standard discrete signals, Properties and their significance (4Hours). Impulse sampling and reconstruction: Sampling theorem (only statement) and reconstruction of signals (2 Hours).</p>	L1, L2, L3
Module -5	
<p>Z-Transforms: Introduction, the Z-transform, properties of the Region of convergence, Properties of the Z-Transform, Inversion of the Z- Transform, Transform analysis of LTI systems.</p>	L1, L2, L3
<p>Course Outcomes: At the end of the course, students will be able to:</p> <ul style="list-style-type: none"> • Identify different types of signals (continuous/discrete, periodic/aperiodic, even /odd, energy/power and deterministic/random signals.) • Identify the linearity, causality, time-invariance and stability properties of continuous and discrete time systems. • Solve the response of a Continuous and Discrete LTI system using convolution integral and convolution sum. • Solve the spectral characteristics of continuous and discrete time signal using Fourier analysis. • Solve Z-transforms, inverse Z-transforms and transfer functions of complex LTI systems. 	
<p>Question paper pattern:</p> <ul style="list-style-type: none"> • The question paper will have ten questions. • Each full Question consisting of 16 marks • There will be 2 full questions (with a maximum of three subquestions) from each module. • Each full question will have subquestions covering all the topics under a module. • The students will have to answer 5 full questions, selecting one full question from each module. 	
<p>Text Book: Simon Haykins and Barry Van Veen, "Signals and Systems", 2nd Edition, 2008, Wiley India. ISBN 9971-51-239-4.</p>	

Reference Books:

1. Michael Roberts, "Fundamentals of Signals & Systems", 2nd edition, Tata McGraw-Hill, 2010, ISBN978-0-07-070221-9.
2. Alan V Oppenheim, Alan S, Willsky and A Hamid Nawab, "Signals and Systems" Pearson Education Asia / PHI, 2nd edition, 1997. Indian Reprint 2002.
3. H. P Hsu, R. Ranjan, "Signals and Systems", Scham's outlines, TMH, 2006.
4. B. P. Lathi, "Linear Systems and Signals", Oxford University Press, 2005.
5. Ganesh Rao and Satish Tunga, "Signals and Systems", Pearson/Sanguine Technical Publishers, 2004.

Web Link and Video Lectures:

1. <https://www.classcentral.com/course/swayam-principles-of-signals-and-systems>
2. <https://freevideolectures.com/subject/signals-systems/>

PRINCIPLES OF COMMUNICATION SYSTEMS
 [As per Choice Based Credit System (CBCS) scheme]
 SEMESTER – IV (EC/TC)

Subject Code	15EC45	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of Lecture Hours	50(10 Hours per Module)	Exam Hours	03
CREDITS – 04			
Course objectives: This course will enable students to: <ul style="list-style-type: none"> • DesignsimplestsystemsforgeneratinganddemodulatingAM,DSB,SSBandVSB signals. • Understandtheconcepts inAnglemodulationforthedesignofcommunication systems. • Designsimplestsystemsforgeneratinganddemodulatingfrequencymodulated signals. • Learn the concepts of random process and varioustypes of noise. • Evaluatetheperformanceofthecommunicationsysteminpresenceofnoise. • Analyzepulse modulation and samplingtechniques. 			
Modules			RBT Level
Module – 1			
AMPLITUDE MODULATION: Introduction, Amplitude Modulation: Time & Frequency – Domain description, Switching modulator, Envelop detector. DOUBLE SIDE BAND-SUPPRESSED CARRIER MODULATION: Time and Frequency – Domain description, Ring modulator, Coherent detection, Costas Receiver, Quadrature Carrier Multiplexing. SINGLE SIDE-BAND AND VESTIGIAL SIDEBAND METHODS OF MODULATION: SSB Modulation, VSB Modulation, FrequencyTranslation, Frequency- Division Multiplexing, Theme Example: VSB Transmission of Analog andDigitalTelevision. (Chapter 3 ofText).			L1, L2, L3
Module – 2			
ANGLE MODULATION: Basic definitions, Frequency Modulation: Narrow Band FM, Wide Band FM, Transmission bandwidth of FM Signals, Generation of FM Signals, Demodulation of FM Signals, FM Stereo Multiplexing, Phase-Locked Loop: Nonlinear model of PLL, Linear model of PLL, Nonlinear Effects in FM Systems. The Superheterodyne Receiver(refer Chapter 4 ofText).			L1, L2, L3
Module – 3			

<p>RANDOM VARIABLES & PROCESS : Introduction, Probability, Conditional Probability, Random variables, Several Random Variables. Statistical Averages: Function of a random variable, Moments, Random Processes, Mean, Correlation and Covariance function: Properties of autocorrelation function, Cross-correlation functions (refer Chapter 5 of Text).</p> <p>NOISE: Shot Noise, Thermal noise, White Noise, Noise Equivalent Bandwidth(referChapter5ofText),NoiseFigure(referSection6.7ofText).</p>	L1, L2, L3
Module – 4	
<p>NOISE IN ANALOG MODULATION: Introduction, Receiver Model, NoiseinDSB-SCreceivers,NoiseinAMreceivers,Thresholdeffect,Noisein FM receivers, Capture effect, FM threshold effect, FM thresholdreduction, Pre-emphasisandDe-emphasisinFM(referChapter6ofText).</p>	L1, L2, L3
Module – 5	
<p>DIGITAL REPRESENTATION OF ANALOG SIGNALS: Introduction, Why Digitize Analog Sources?, The Sampling process, Pulse Amplitude Modulation, Time Division Multiplexing, Pulse-Position Modulation, Generation of PPM Waves, Detection of PPM Waves, The Quantization Process, Quantization Noise, Pulse-Code Modulation: Sampling, Quantization, Encoding, Regeneration, Decoding, Filtering, Multiplexing (refer Chapter 7 of Text), Application to Vocoder (refer Section 6.8 of Reference Book 1).</p>	L1, L2, L3
<p>Course Outcomes: At the end of the course, students will be able to:</p> <ul style="list-style-type: none"> • Apply the time and frequency domain knowledge for the generation and demodulation of amplitude modulated signals. • Identify the performance of different generation and detection methodologies of AM, FM and multiplexing. • Utilize analog signals in time domain as random processes and identify the types of basic Noise • Identify the influence of noise in receivers of analog modulated signals • Compare the characteristics of pulse modulation techniques 	
<p>Question paper pattern:</p> <ul style="list-style-type: none"> • The question paper will have tenquestions. • Each full Question consisting of 16marks. • Therewillbe2fullquestions(withamaximumofThreesubquestions)fromeach module. • Eachfullquestionwillhavesubquestionscoveringallthetopicsunderamodule. • Thestudentswillhavetoanswer5fullquestions,selectingonefullquestionfrom eachmodule. 	
<p>Text Book:</p> <p>Communication Systems , Simon Haykins&Moher, 5th Edition, John Willey, India Pvt. Ltd, 2010, ISBN 978 – 81 – 265 – 2151 – 7.</p>	
Reference Books:	

1. Modern Digital and Analog Communication Systems, B. P. Lathi, Oxford University Press., 4thedition.
2. An Introduction to Analog and Digital Communication , Simon Haykins, John Wiley India Pvt. Ltd., 2008, ISBN978–81–265–3653–5.
3. PrinciplesofCommunicationSystems,H.Taub&D.L.Schilling,TMH, 2011.
4. CommunicationSystems,HaroldP.E,SternSamyandA.Mahmond,Pearson Edition,2004.
5. Communication Systems :Analog and Digital, R.P.Singh and S.Sapre: TMH 2ndedition,2007.

Web Link and Video Lectures:

1. https://swayam.gov.in/nd1_noc19_ee46/preview
2. <https://www.udemy.com/course/analog-communication/>

<u>LINEAR INTEGRATED CIRCUITS</u> [As per Choice Based Credit System (CBCS) scheme] SEMESTER – IV (EC/TC)			
Subject Code	15EC46	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of Lecture Hours	50(10 Hours per Module)	Exam Hours	03
CREDITS – 04			
<p>Course objectives: This course will enable students to:</p> <ul style="list-style-type: none"> • Define and describe various parameters of Op-Amp, its characteristics and specifications. • Discuss the effects of Input and Output voltage ranges upon Op-Amp circuits. • Sketch and Analyze Op-Amp circuits to determine Input Impedances, output Impedances and other performance parameters. • Sketch and Explain typical Frequency Response graphs for each of the Filter circuits showing Butterworth and Chebyshev responses where ever appropriate. • Describe and Sketch the various switching circuits of Op-Amps and analyze its operations. • Differentiate between various types of DACs and ADCs and evaluate the performance of each with neat circuit diagrams and assuming suitable inputs. 			
Modules			RBT Level
Module -1			
<p>Operational Amplifier Fundamentals: Basic Op-amp circuit, Op-Amp parameters – Input and output voltage, CMRR and PSRR, offset voltages and currents, Input and output impedances, Slew rate and Frequency limitations. OP-Amps as DC Amplifiers – Biasing OP-amps, Direct coupled voltage followers, Non- inverting amplifiers, inverting amplifiers, Summing amplifiers, and Difference amplifiers. Interpretation of OP-amp LM741 & TL081 datasheet.(Text1)</p>			L1, L2,L3
Module -2			
<p>Op-Amps as AC Amplifiers: Capacitor coupled voltage follower, High input impedance– Capacitor coupled voltage follower, Capacitor coupled non inverting amplifiers, High input impedance – Capacitor coupled Non inverting amplifiers, Capacitor coupled inverting amplifiers, setting the upper cut-off frequency, Capacitor coupled difference amplifier. OP-Amp Applications: Voltage sources, current sources and current sinks, current amplifiers, instrumentation amplifier, precision rectifiers.(Text1)</p>			L1, L2,L3
Module-3			

More Applications : Limiting circuits, Clamping circuits, Peakdetectors, Sample and hold circuits, V to I and I to V converters, Differentiating Circuit, Integrator Circuit, Phase shift oscillator, Wien bridge oscillator, Crossing detectors, inverting Schmitt trigger. (Text 1)
Log and antilog amplifiers, Multiplier and divider. (Text2)

L1, L2,L3

Module -4	
Active Filters: First order and second order active Low-pass and high pass filters, Bandpass Filter, Bandstop Filter. (Text 1) Voltage Regulators: Introduction, Series Op-amp regulator, IC voltage regulators. 723 general purpose regulators. (Text 2)	L1, L2, L3
Module -5	
Phase locked loop: Basic Principles, Phase detector/comparator, VCO. DAC and ADC convertor: DAC using R-2R, ADC using Successive approximation. Other IC Application: 555 timer, Basic timer circuit, 555 timer used as astable and monostable multivibrator. (Text 2)	L1, L2, L3
<p>Course Outcomes: After studying this course, students will be able to:</p> <ul style="list-style-type: none"> • Identify Op-amp circuit and parameters including CMRR, PSRR, Input & Output Impedances and Slew Rate. • Construct Op-amp based AC Amplifiers and Develop circuits for Op-amp based Voltage / Current Sources & Sinks, Current, Instrumentation and Precision Amplifiers. • Develop circuits for Op Amp based linear and non-linear circuits comprising of limiting, clamping, Sample & Hold, Differentiator / Integrator Circuits, Peak Detectors, Oscillators and Multiplier & Divider. • Design first & Second Order Filters and Voltage Regulators. • Illustrate applications of linear ICs in phase detector, VCO, DAC, ADC and Timer. 	
<p>Question paper pattern:</p> <ul style="list-style-type: none"> • The question paper will have ten questions. • Each full Question consisting of 16 marks. • There will be 2 full questions (with a maximum of three subquestions) from each module. • Each full question will have subquestions covering all the topics under a module. • The students will have to answer 5 full questions, selecting one full question from each module. 	
<p>Text Books:</p> <ol style="list-style-type: none"> 1. "Operational Amplifiers and Linear IC's", David A. Bell, 2nd edition, PHI/Pearson, 2004. ISBN 978-81-203-2359-9. 2. "Linear Integrated Circuits", D. Roy Choudhury and Shail B. Jain, 4th edition, Reprint 2006, New Age International ISBN 978-81-224-3098-1. 	

Reference Books:

1. RamakantAGayakwad, "Op-Amps and Linear Integrated Circuits", Pearson, 4th Ed, 2015. ISBN 81-7808-501-1.
2. BSomanathanNair, "Linear Integrated Circuits: Analysis, Design & Applications," Wiley India, 1st Edition, 2015.
3. JamesCox, "Linear Electronics Circuits and Devices", Cengage Learning, Indian Edition, 2008, ISBN-13: 978-07-668-3018-7.
4. Data Sheet: <http://www.ti.com/lit/ds/symlink/tl081.pdf>.

Web Link and Video Lectures:

1. <https://e-box.co.in/linear-integrated-circuits.shtml>
2. <https://freevidelectures.com/course/2915/linear-integrated-circuits>

MICROPROCESSOR LABORATORY

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER – IV (EC/TC)

Laboratory Code	15ECL47	IA Marks	20
Number of Lecture Hours/Week	01Hr Tutorial (Instructions) + 02 Hours Laboratory	Exam Marks	80
RBT Level	L1, L2, L3	Exam Hours	03

CREDITS – 02

Course objectives: This course will enable students to:

- Get familiarized with 8086 instructions and DOS 2.1 interrupts and function calls.
- Develop and test assembly language programs using instructions of 8086.
- Get familiarized with interfacing of various peripheral devices with 8086 microprocessor for simple applications.

Laboratory Experiments:

1. Programs involving:

Data transfer instructions like :

- i) Byte and word data transfer in different addressing Modes
- ii) Block move (with and without overlap)
- iii) Block interchange

2. Programs involving :

Arithmetic & logical operations like :

- i) Addition and Subtraction of multi precision nos.
- ii) Multiplication and Division of signed and unsigned Hexadecimal nos.
- iii) ASCII adjustment instructions.
- iv) Code conversions.

3. Programs involving:

Bit manipulation instructions like checking:

- i) Whether given data is positive or negative
- ii) Whether given data is odd or even
- iii) Logical 1's and 0's in given data
- iv) 2 out of 5 code
- v) Bit wise and nibble wise palindrome

4. Programs involving:

Branch/ Loop instructions like

- i) Arrays: addition/subtraction of N nos., Finding largest and smallest nos., Ascending and descending order.
- ii) Two application programs using Procedures and Macros (Subroutines).

<p>5. Programs involving String manipulation like string transfer, string reversing, searching for a string.</p>
<p>6. Programs involving ProgramstouseDOSinterruptINT21hFunctioncallsforReadingaCharacterfrom keyboard,BufferedKeyboardinput,Displayofcharacter/Stringonconsole.</p>
<p>7. Interfacing Experiments :</p> <p>Experimentsoninterfacing8086withthefollowinginterfacingmodulesthroughDIO (DigitalInput/Output- PCibuscompatiblecard/8086Trainer)</p> <ol style="list-style-type: none"> 1. Matrix keyboardinterfacing 2. Seven segment displayinterface 3. Logical controllerinterface 4. Stepper motorinterface 5. ADC and DAC Interface (8bit) 6. Lightdependentresistor(LDR),Relayand BuzzerInterfacetomakelight operated switches
<p>Course Outcomes: On the completion of this laboratory course, the students will be able to:</p> <ul style="list-style-type: none"> • Identify the different CPU architectures, 8086 Microprocessor architecture and addressing modes of 8086. • Make use of the instruction set and addressing modes of 8086 to develop assembly language programs • Make use of stacks , interrupts to develop programs. • Model the static memory chips, 8255 & 8254, and use of INT 21 DOS interrupt function calls to handle keyboard and display • Experiment with 8086 Microprocessor to interface the ADC-0808, DAC-0800 and stepper motor using PPI 8255.
<p>Conduct of Practical Examination:</p> <ul style="list-style-type: none"> • Alllaboratoryexperimentsaretobeincludedforpracticalexamination. • Forexamination,onequestionfromsoftwareandonequestionfromhardware interfacing to beset. • Students are allowed to pick one experiment from thelot. • ChangeofexperimentisallowedonlyonceandMarksallottedtotheprocedure part to be madezero.

LINEAR ICS AND COMMUNICATION LAB
As per Choice Based Credit System (CBCS) scheme]
SEMESTER – IV (EC/TC)

Laboratory Code	15ECL48	IA Marks	20
Number of Lecture Hours/Week	01Hr Tutorial (Instructions) + 02 Hours Laboratory	Exam Marks	80
RBT Level	L1, L2, L3	Exam Hours	03

CREDITS – 02

- Course objectives: This laboratory course enables students to:
- Design, Demonstrate and Analyze instrumentation amplifier, filters, DAC, adder, differentiator and integrator circuits, using op-amp.
 - Design, Demonstrate and Analyze multivibrators and oscillator circuits using Op-amp
 - Design, Demonstrate and Analyze analog systems for AM, FM and Mixer operations.
 - Design, Demonstrate and Analyze balance modulation and frequency synthesis.
 - Demonstrate and Analyze pulse sampling and flat top sampling.

Laboratory Experiments:

1. Design an instrumentation amplifier of a differential mode gain of 'A' using three amplifiers.

2. Design of RC Phase shift and Wien's bridge oscillators using Op-amp.

3. Design active second order Butterworth low pass and high pass filters.

4. Design 4bit R-2R Op-Amp Digital to Analog Converter (i) using 4bit binary input from toggle switches and (ii) by generating digital inputs using mod-16 counter.

5. Design Adder, Integrator and Differentiator using Op-Amp.

6. Design of Monostable and Astable Multivibrator using 555 Timer.

7. Demonstrate Pulse sampling, flat top sampling and reconstruction.

8. Amplitude modulation using transistor/FET (Generation and detection).

9. Frequency modulation using IC 8038/2206 and demodulation.

10. Design BJT/FET Mixer.

11. DSBSC generation using Balance Modulator IC 1496/1596.

12. Frequency synthesis using PLL.

Conduct of Practical Examination:

- All laboratory experiments are to be included for practical examination.
- Students are allowed to pick one experiment from the lot.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

Course Outcomes: This laboratory course enables students to:

- Inspect the basic analog systems for a given specification using the basic building blocks and ICs.
- Examine the performance of instrumentation amplifier, LPF, HPF, DAC and oscillators using linear IC.
- Analyze with Linear ICs for applications like addition, integration, differentiation and 555 timer operations to generate pulses.
- Test for pulse and flat top sampling techniques.
- Experiment with Amplitude and Frequency Modulation techniques to find the percentage of modulation and use PLL to synthesize the Frequency.

B.E E&C SIXTH SEMESTERSYLLABUS

DIGITALCOMMUNICATION

B.E., VI Semester, Electronics &Communication Engineering/
TelecommunicationEngineering
[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC61	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of Lecture Hours	50 (10Hours/Module)	Exam Hours	03

CREDITS – 04

Course Objectives: The objectives of the course is to enable students to:

- Understand the mathematical representation of signal, symbol, noise and channels.
- Apply the concept of signal conversion to symbols and signal processing to symbols in transmitter and receiver functionalblocks.
- Compute performance issues and parameters for symbol processing and recovery in ideal and corrupted channelconditions.
- Compute performance parameters and mitigate for these parameters in corrupted and distorted channelconditions.

Module-1	RBT Level
<p>Bandpass Signal to Equivalent Low pass: Hilbert Transform, Pre- envelopes, Complex envelopes, Canonical representation of bandpass signals, Complex low pass representation of bandpass systems, Complex representation of band pass signals and systems (Text 1: 2.8, 2.9, 2.10, 2.11, 2.12, 2.13).</p> <p>Line codes: Unipolar, Polar, Bipolar (AMI) and Manchester code and their power spectral densities (Text 1: Ch 6.10).</p> <p>Overview of HDB3, B3ZS, B6ZS (Ref. 1: 7.2)</p>	L1, L2, L3
Module-2	
<p>SignalingoverAWGNChannels-Introduction,Geometricrepresentationof signals, Gram-Schmidt Orthogonalization procedure, Conversion of the continuousAWGNchannelintoavectorchannel,Optimumreceiversusing coherent detection: ML Decoding, Correlation receiver, matched filter receiver (Text 1: 7.1, 7.2, 7.3,7.4).</p>	L1, L2, L3
Module-3	
<p>Digital Modulation Techniques : Phase shift Keying techniques using coherent detection: generation, detection and error probabilities of BPSK and QPSK, M-ary PSK, M-ary QAM (Relevant topics in Text 1 of 7.6, 7.7).</p> <p>Frequency shift keying techniques using Coherent detection: BFSK</p>	

<p>generation, detection and error probability (Relevant topics in Text 1 of 7.8).</p> <p>Non coherent orthogonal modulation techniques: BFSK, DPSK Symbol representation, Block diagrams treatment of Transmitter and Receiver, Probability of error (without derivation of probability of error equation)(Text 1: 7.11, 7.12.7.13).</p>	
Module-4	
<p>Communication through Band Limited Channels : Digital Transmission through Band limited channels: Digital PAM Transmission through Band limited Channels, Signal design for Band limited Channels: Design of band limited signals for zero ISI–The Nyquist Criterion (statement only), Design of band limited signals with controlled ISI-Partial Response signals, Probability of error for detection of Digital PAM: Probability of error for detection of Digital PAM with Zero ISI, Symbol-by-Symbol detection of data with controlled ISI (Text 2: 9.1, 9.2, 9.3.1, 9.3.2).</p> <p>Channel Equalization: Linear Equalizers (ZFE, MMSE), Adaptive Equalizers (Text 2: 9.4.2).</p>	L1, L2, L3
Module-5	
<p>Principles of Spread Spectrum: Spread Spectrum Communication Systems: Model of a Spread Spectrum Digital Communication System, Direct Sequence Spread Spectrum Systems, Effect of De-spreading on a narrowband Interference, Probability of error (statement only), Some applications of DS Spread Spectrum Signals, Generation of PN Sequences, Frequency Hopped Spread Spectrum, CDMA based on IS-95 (Text 2: 11.3.1, 11.3.2, 11.3.3, 11.3.4, 11.3.5, 11.4.2).</p>	L1, L2, L3
<p>Course Outcomes: At the end of the course, the students will be able to:</p> <ul style="list-style-type: none"> • Develop the concepts of Band pass sampling to well specified signals and channels. • Utilize performance parameters and transfer rates for low pass and bandpass symbol under ideal and corrupted non band limited channels. • Identify valid symbol processing and performance parameters at the receiver under ideal and corrupted band limited channels. • Identify the bandpass signals when subjected to corruption and distortion during transmission over a band limited channel. • Identify the need for data security using spread spectrum technique and error rate calculation. 	
<p>Question paper pattern:</p> <ul style="list-style-type: none"> • The question paper will have ten questions • Each full question consists of 16 marks. • There will be 2 full questions (with a maximum of three subquestions) from each module. • Each full question will have subquestions covering all the topics under a module • The students will have to answer 5 full questions, selecting one full question from each module 	
Text Books:	

1. Simon Haykin, "Digital Communication Systems", John Wiley & sons, First Edition, 2014, ISBN978-0-471-64735-5.
2. John G Proakis and Masoud Salehi, "Fundamentals of Communication Systems", 2014 Edition, Pearson Education, ISBN978-8-131-70573-5.

Reference Books:

1. B.P.Lathi and Zhi Ding, "Modern Digital and Analog communication Systems", Oxford University Press, 4th Edition, 2010, ISBN:978-0-198-07380-2.
2. Ian A Glover and Peter M Grant, "Digital Communications", Pearson Education, Third Edition, 2010, ISBN978-0-273-71830-7.
3. John G Proakis and Masoud Salehi, "Communication Systems Engineering", 2nd Edition, Pearson Education, ISBN978-93-325-5513-6.

Web Link and Video Lectures:

1. <https://www.classcentral.com/course/swayam-modern-digital-communication-techniques>
2. <https://nptel.ac.in/courses/117/101/117101051/>

ARM MICROCONTROLLER & EMBEDDED SYSTEMS

B.E., VI Semester, Electronics & Communication Engineering/ Telecommunication Engineering
[As per Choice Based Credit System (CBCS) scheme]

<u>ARM MICROCONTROLLER & EMBEDDED SYSTEMS</u>			
B.E., VI Semester, Electronics & Communication Engineering/ Telecommunication Engineering [As per Choice Based Credit System (CBCS) Scheme]			
Course Code	15EC62	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of Lecture Hours	50 (10 Hours / Module)	Exam Hours	03
CREDITS – 04			
Course objectives: This course will enable students to:			
<ul style="list-style-type: none">• Understand the architectural features and instruction set of 32-bit microcontroller ARM Cortex M3.• Program ARM Cortex M3 using the various instructions and C language for different applications.• Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.• Develop the hardware software co-design and firmware design approaches.• Explain the need of real-time operating system for embedded system applications.			
Module-1			
ARM-32bit Microcontroller: Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, Debugging support, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence (Text 1: Ch 1, 2, 3) L1, L2			
Module-2			
ARM Cortex M3 Instruction Sets and Programming: Assembly basics, Instruction list and description, Useful instructions, Memory mapping, Bit-band operations and CMSIS, Assembly and C language Programming (Text 1: Ch-4, Ch-5, Ch-10(10.1, 10.2, 10.3, 10.5 only) L1, L2, L3			
Module-3			
Embedded System Components: Embedded Vs General computing system, Classification of Embedded systems, Major applications and purpose of ES. Core of an Embedded System including all types of processor/controller, Memory, Sensors, Actuators, LED, 7 segment LED display, Optocoupler, Relay, Piezo buzzer, Push button switch, Communication Interface (onboard and external types), Embedded firmware, Other system components. (Text 2: All the Topics from Ch-1 and Ch-2, excluding 2.3.3.4 (stepper motor), 2.3.3.8 (keyboard) and 2.3.3.9 (PPI) sections). L1, L2, L3			
Module-4			
Embedded System Design Concepts : Characteristics and Quality Attributes of Embedded Systems, Operational and non-operational quality attributes, Embedded			

Systems-Application and Domain specific, Hardware Software Co-Design and Program Modelling (excluding UML), Embedded firmware design and development (excluding C language).
(Text 2: Ch-3, Ch-4, Ch-7 (Sections 7.1, 7.2 only), Ch-9 (Sections 9.1, 9.2, 9.3.1, 9.3.2 only) L1, L2, L3

Module-5

RTOS and IDE for Embedded System Design: Operating System basics, Types of operating systems, Task, process and threads (Only POSIX threads with an example program), Thread preemption, Preemptive Task scheduling techniques, Task Communication, Task synchronization issues – Racing and Deadlock, Concept of Binary and counting semaphores (Mutex example without any program), How to choose an RTOS, Integration and testing of Embedded hardware and firmware, Embedded system Development Environment – Block diagram (excluding Keil),
Disassembler/decompiler, simulator, emulator and debugging techniques
(Text 2: Ch-10 (Sections 10.1, 10.2, 10.3, 10.5.2, 10.7, 10.8.1.1, 10.8.1.2, 10.8.2.2, 10.10 only), Ch 12, Ch-13 (a block diagram before 13.1, 13.3, 13.4, 13.5, 13.6 only)
L1, L2, L3

Course outcomes: After studying this course, students will be able to:

- Construct the architectural features and instructions of 32 bit microcontroller ARM Cortex M3.
- Make use of the knowledge gained for Programming ARM Cortex M3 for different applications.
- Identify the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
- Develop the hardware/software co-design and firmware design using ARM Cortex M3 Instruction set.
- Analyze the need of real time operating system for embedded system applications

Text Books :

1. Joseph Yiu, “The Definitive Guide to the ARM Cortex-M3”, 2nd Edition, Newnes, (Elsevier), 2010.
2. Shibu K V, “Introduction to Embedded Systems”, Tata McGraw Hill Education Private Limited, 2nd Edition.

Web Link and Video Lectures:

1. <https://nptel.ac.in/courses/117/106/117106111/>
2. <https://www.classcentral.com/course/swayam-embedded-system-design-with-arm>

VLSI Design

B.E., VI Semester, Electronics & Communication Engineering
[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC63	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of LectureHours	50 (10 Hours / Module)	Exam Hours	03
CREDITS – 04			
<p>Course Objectives: The objectives of the course is to enable students to:</p> <ul style="list-style-type: none"> • Impart knowledge of MOS transistor theory and CMOS technologies • Impart knowledge on architectural choices and performance tradeoffs involved in designing and realizing the circuits in CMOS technology • Cultivate the concepts of subsystem design processes • Demonstrate the concepts of CMOS testing 			
Module-1			RBT Level
<p>Introduction : A Brief History, MOS Transistors, MOS Transistor Theory, Ideal I-V Characteristics, Non-ideal I-V Effects, DC Transfer Characteristics (1.1, 1.3, 2.1, 2.2, 2.4, 2.5 of TEXT2). Fabrication: nMOS Fabrication, CMOS Fabrication [P-well process, N-well process, Twin tub process], BiCMOS Technology (1.7, 1.8, 1.10 of TEXT1).</p>			L1, L2
Module-2			
<p>MOS and BiCMOS Circuit Design Processes : MOS Layers, Stick Diagrams, Design Rules and Layout. Basic Circuit Concepts: Sheet Resistance, Area Capacitances of Layers, Standard Unit of Capacitance, Some Area Capacitance Calculations, Delay Unit, Inverter Delays, Driving Large Capacitive Loads (3.1 to 3.3, 4.1, 4.3 to 4.8 of TEXT1).</p>			L1, L2, L3
Module-3			
<p>Scaling of MOS Circuits: Scaling Models & Scaling Factors for Device Parameters Subsystem Design Processes: Some General considerations, An illustration of Design Processes, Illustration of the Design Processes - Regularity, Design of an ALU Subsystem, The Manchester Carry-chain and Adder Enhancement Techniques (5.1, 5.2, 7.1, 7.2, 8.2, 8.3, 8.4.1, 8.4.2 of TEXT1).</p>			L1, L2, L3
Module-4			
<p>Subsystem Design: Some Architectural Issues, Switch Logic, Gate (restoring) Logic, Parity Generators, Multiplexers, The Programmable Logic Array (PLA) (6.1 to 6.3, 6.4.1, 6.4.3, 6.4.6 of TEXT1). FPGA Based Systems: Introduction, Basic concepts, Digital design and FPGA's, FPGA based System design, FPGA architecture, Physical design for FPGA's (1.1 to 1.4, 3.2, 4.8 of TEXT3).</p>			L1, L2, L3
Module-5			
<p>Memory, Registers and Aspects of system Timing - System Timing Considerations, Some commonly used Storage/Memory elements (9.1, 9.2 of TEXT1).</p>			L1, L2, L3

Testing and Verification: Introduction, Logic Verification, Logic Verification Principles, Manufacturing Test Principles, Design for testability (12.1, 12.1.1, 12.3, 12.5, 12.6 of TEXT2).

Course outcomes: At the end of the course, the students will be able to:

- Utilize the concept of basic MOS transistor, CMOS fabrication flow and technology scaling.
- Make use of the knowledge of physical design aspects to make stick and layout diagrams for various gates.
- Identify the concept of Memory elements along with timing considerations with scaling fundamentals
- Experiment with the basic knowledge of FPGA based system design and testability issues in VLSI Design
- Analyze the various CMOS subsystems and architectural issues with the design constraints.

Question paper pattern:

- The question paper will have ten questions
- Each full question consists of 16 marks.
- There will be 2 full questions (with a maximum of three subquestions) from each module.
- Each full question will have subquestions covering all the topics under a module
- The students will have to answer 5 full questions, selecting one full question from each module

Text Books:

1. "Basic VLSI Design" - Douglas A. Pucknell & Kamran Eshraghian, PHI 3rd Edition (original Edition – 1994).
2. "CMOS VLSI Design- A Circuits and Systems Perspective"- Neil H.E. Weste, David Harris, Ayan Banerjee, 3rd Edition, Pearson Education.
3. "FPGA Based System Design"- Wayne Wolf, Pearson Education, 2004, Technology and Engineering.

Web Link and Video Lectures:

1. <https://www.coursera.org/learn/vlsi-cad-logic>
2. <https://www.classcentral.com/tag/vlsi-design>

COMPUTER COMMUNICATION NETWORKS

B.E., VI Semester, Electronics & Communication Engineering / Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

<u>COMPUTER COMMUNICATION NETWORKS</u> B.E., VI Semester, Electronics & Communication Engineering / Telecommunication Engineering [As per Choice Based Credit System (CBCS) Scheme]			
Course Code	15EC64	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of Lecture Hours	50 (10 Hours /Module)	Exam Hours	03
CREDITS – 04			
Course Objectives: This course will enable students to: <ul style="list-style-type: none">• Understand the layering architecture of OSI reference model and TCP/IP protocol suite.• Understand the protocols associated with each layer.• Learn the different networking architectures and their representations.• Learn the various routing techniques and the transport layer services.			
Module-1			
Introduction: Data Communications: Components, Representations, Data Flow, Networks: Physical Structures, Network Types: LAN, WAN, Switching, Internet. Network Models: Protocol Layering: Scenarios, Principles, Logical Connections, TCP/IP Protocol Suite: Layered Architecture, Layers in TCP/IP suite, Description of layers, Encapsulation and Decapsulation, Addressing, Multiplexing and Demultiplexing, The OSI Model: OSI Versus TCP/IP. Data-Link Layer: Introduction: Nodes and Links, Services, Categories' of link, Sublayers, Link Layer addressing: Types of addresses, ARP. Data Link Control(DLC) services: Framing, Flow and Error Control, Data Link Layer Protocols: Simple Protocol, Stop and Wait protocol, Piggybacking. L1, L2			
Module-2			
Media Access Control: Random Access: ALOHA, CSMA, CSMA/CD, CSMA/CA. Controlled Access: Reservation, Polling, Token Passing. Wired LANs: Ethernet: Ethernet Protocol: IEEE802, Ethernet Evolution, Standard Ethernet: Characteristics, Addressing, Access Method, Efficiency, Implementation, Fast Ethernet: Access Method, Physical Layer, Gigabit Ethernet: MAC Sublayer, Physical Layer, 10 Gigabit Ethernet. L1, L2			
Module-3			
Wireless LANs: Introduction: Architectural Comparison, Characteristics, IEEE802.11: Architecture, MAC Sublayer, Addressing Mechanism, Physical Layer, Bluetooth: Architecture, Layers. Connecting Devices: Hubs, Switches, Virtual LANs: Membership, Configuration, Communication between Switches and Routers, Advantages. Network Layer: Introduction, Network Layer services: Packetizing, Routing and Forwarding, Other services, Packet Switching: Datagram Approach, Virtual Circuit Approach, IPV4 Addresses: Address Space, Classful Addressing, Classless Addressing.			

DHCP, Network Address Resolution, Forwarding of IP Packets: Based on destination Address and Label. L1, L2

Module-4

Network Layer Protocols: Internet Protocol (IP): Datagram Format, Fragmentation, Options, Security of IPv4 Datagrams, ICMPv4: Messages, Debugging Tools, MobileIP: Addressing, Agents, Three Phases, Inefficiency in MobileIP.

Unicast Routing: Introduction, Routing Algorithms: Distance Vector Routing, Link State Routing, Path vector routing, Unicast Routing Protocol: Internet Structure, Routing Information Protocol, Open Shortest Path First, Border Gateway Protocol

Version 4. L1, L2, L3

Module-5

Transport Layer: Introduction: Transport Layer Services, Connectionless and Connection oriented Protocols, Transport Layer Protocols: Simple protocol, Stop and wait protocol, Go-Back-N Protocol, Selective repeat protocol, User Datagram Protocol:

User Datagram, UDP Services, UDP Applications, Transmission Control Protocol: TCP Services, TCP Features, Segment, Connection, State Transition diagram, Windows in TCP, Flow control, Error control, TCP congestion control. L1, L2

Course Outcomes: At the end of the course, the students will be able to:

- Make use of the layering architecture of computer networks and distinguish between the OSI reference model and TCP/IP protocol suite.
- Identify the protocols and services of Data link layer
- Identify the protocols and functions associated with the transport layer services.
- Construct a network model and determine the routing of packets using different routing algorithms.
- Distinguish the basic network configurations and standards associated with each network.

Text Book:

Data Communications and Networking , Forouzan, 5th Edition, McGraw Hill, 2016 ISBN: 1-25-906475-3

Reference Books:

1. Computer Networks, James JKurose, Keith WRoss, Pearson Education, 2013, ISBN:0-273-76896-4
2. Introduction to Data Communication and Networking, Wayarles Tomasi, Pearson Education, 2007, ISBN:0130138282

Web Link and Video Lectures:

1. <https://www.classcentral.com/course/fundamentals-network-communications>
2. <https://www.udacity.com/course/computer-networking--ud436>

CELLULAR MOBILE COMMUNICATIONS

B.E., VI Semester, Electronics & Communication Engineering/ Telecommunication Engineering
[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC651	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (8 Hours /Module)	Exam Hours	03
CREDITS – 03			
<p>Course Objectives: This course enables students to:</p> <ul style="list-style-type: none"> • Understand the application of multiuser access in a cellular communication scenario. • Understand the propagation mechanisms in an urban mobile communications using statistical and empirical models. • Understand system architecture, call processing protocols and services of GSM, GPRS and EDGE. • Understand system architecture, call processing protocols and services of CDMA based systems IS95 and CDMA2000. 			

Module-1	RBT Level
<p>Cellular Concept: Frequency Reuse, Channel Assignment Strategies, Interference and System Capacity, Power Control for Reducing Interference, Trunking and Grade of Service, Improving Capacity in Cellular Systems.</p> <p>Mobile Radio Propagation: Large Scale path Loss- Free Space Model, Three basic propagation mechanisms, Practical Link Budget Design using Path Loss Models, Outdoor Propagation Models – Okumura, Hata, PCSE extension to Hata Model (explanations only) (Text 1).</p>	L1, L2
Module-2	
<p>Mobile Radio Propagation: Small -Scale Fading and Multipath: Small scale Multipath Propagation, Impulse Response Model of a Multipath Channel, Small-Scale Multipath Measurements, Parameters of Mobile Multipath Channels, Types of Small-Scale Fading, Rayleigh and Ricean Distributions, Statistical Model for Multipath Fading Channels (Clarke’s Model for Flat Fading only). (Text 1)</p>	L1, L2
Module-3	
<p>System Architecture and Addressing : System architecture, The SIM concept, Addressing, Registers and subscriber data, Location registers (HLR and VLR) Security-related registers (AUC and EIR), Subscriber data, Network interfaces and configurations.</p> <p>Air Interface – GSM Physical Layer: Logical channels, Physical channels, Synchronization- Frequency and clock synchronization, Adaptive frame synchronization, Mapping of logical onto physical channels, Radio subsystem link control, Channel coding, source coding and speech processing, Source coding and speech processing, Channel coding, Power-up scenario.</p> <p>GSM Protocols: Protocol architecture planes, Protocol architecture of the user plane, Protocol architecture of the signaling plane, Signaling at the air interface (Um), Signaling at the A and Abis interfaces, Security-related network functions,</p>	L1, L2

Signaling at the user interface.(Text 2)	
Module-4	
<p>GSM Roaming Scenarios and Handover : Mobile application part interfaces, Location registration and location update, Connection establishment and termination, Handover. (up to 6.4.1 only in Text2)</p> <p>Services: Classical GSM services, Popular GSM services: SMS and MMS. Improved data services in GSM : GPRS, HSCSD and EDGE GPRS System architecture of GPRS, Services, Session management, mobility management and routing, Protocol architecture, Signaling plane, Interworking with IP networks, Air interface, Authentication and ciphering, Summary of GPRS. HSCSD: Architecture, Air interface, HSCSD resource allocation and capacity issues. EDGE: The EDGE concept, EDGE physical layer, modulation and coding, EDGE: effects on the GSM system architecture, ECSD and EGPRS. (Text 2)</p>	L1, L2
Module-5	
<p>CDMA Technology – Introduction to CDMA, CDMA frequency bands, CDMA Network and System Architecture, CDMA Channel concept, Forward Logical Channels, Reverse logical Channels, CDMA frame format, CDMA System Operations (Initialization/Registration), Call Establishment, CDMA Call handoff, IS-95B, CDMA2000, W-CDMA, UMTS, CDMA data networks, Evolution of CDMA to 3G, CDMA 2000 RAN Components, CDMA 2000 Packet Data Service. (Text 3)</p>	L1, L2
<p>Course outcomes: At the end of the course, the students will be able to:</p> <ul style="list-style-type: none"> • Identify the statistical characterization of urban mobile channels to compute the performance for simple modulation schemes. • Identify the functionalities of GSM, GPRS and CDMA to meet high data rate requirements and limited improvements that are needed • Analyse the call process procedure between a calling number and called number for all scenarios in GSM or CDMA based systems • Build and validate voice / data call handling for various scenarios in GSM and CDMA systems for national and international interworking situations • Choose voice and data call handling for various scenarios CDMA systems for national and international interworking situations 	
<p>Question paper pattern:</p> <ul style="list-style-type: none"> • The question paper will have ten questions • Each full question consists of 16 marks. • There will be 2 full questions (with a maximum of three subquestions) from each module. • Each full question will have subquestions covering all the topics under a module • The students will have to answer 5 full questions, selecting one full question from each module 	
<p>Text Books:</p> <ol style="list-style-type: none"> 1. Theodore Rappoport, “Wireless Communications – Principles and Practice”, Prentice Hall of India , 2nd Edition, 2007, ISBN 978-8-120-32381-0. 2. Jorg Eberspacher, Hans-Jorg Vogel, Christian Bettstetter, Christian Hartmann, 	

"GSM–Architecture,ProtocolsandServices”,Wiley,3rdEdition,2009,ISBN-978- 0-470-03070-7.

3. Gary J Mullet, “Introduction To Wireless Telecommunications Systems and Networks”, Cengage Learning.

ADAPTIVE SIGNAL PROCESSING

B.E., VI Semester, Electronics & Communication Engineering/ Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC652	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (8 Hours /Module)	Exam Hours	03
CREDITS – 03			
<p>Course Objectives: The objectives of this course are to:</p> <ul style="list-style-type: none"> • Introduce to the concept and need of adaptive filters and popular adaptive signal processing algorithms • Understand the concepts of training and convergence and the trade-off between performance and complexity. • Introduce to common linear estimation techniques • Demonstrate applications of adaptive systems to sample problems. • Introduce inverse adaptive modelling. 			
Module-1			RBT Level
Adaptive systems: Definitions and characteristics - applications – properties-examples - adaptive linear combiner input signal and weight vectors-performance function- gradient and minimum mean square error- introduction to filtering-smoothing and prediction- linear optimum filtering- orthogonality-Wiener-Hopfequation-performance surface(Chapters 1&2 of Text).			L1, L2
Module-2			
Searching performance surface -stability and rate of convergence : Learning curve-gradient search - Newton's method - method of steepest descent - comparison - Gradient estimation - performance penalty-variance -excess MSE and time constants – mis-adjustments(Chapters 4&5 of Text).			L1, L2
Module-3			
LMS algorithm convergence of weight vector: LMS/Newton algorithm - properties - sequential regression algorithm - adaptive recursive filters - random-search algorithms - lattice structure - adaptive filters with orthogonal signals (Chapters 6& 8 of Text).			L1, L2, L3
Module-4			
Applications-adaptive modeling and system identification : Multipath communication channel, geophysical exploration, FIR digital filters synthesis. (Chapter 9 of Text).			L1, L2, L3
Module-5			
Inverse adaptive modeling : Equalization, and deconvolution adaptive equalization of telephone channels-adapting poles and zeros for IIR digital filter synthesis(Chapter 10 of Text).			L1, L2, L3
<p>Course Outcomes: At the end of the course, students should be able to:</p> <ul style="list-style-type: none"> • Devise filtering solutions for optimising the cost function indicating error in estimation of parameters and appreciate the need for adaptation in design. • Evaluate the performance of various methods for designing adaptive filters 			

through estimation of different parameters of stationary random process clearly considering practical application specifications.

- Analyse convergence and stability issues associated with adaptive filter design and come up with optimum solutions for real life applications taking care of requirements in terms of complexity and accuracy.
- Design and implement filtering solutions for applications such as channel equalisation, interference cancelling and prediction considering present day challenges.

Question paper pattern:

- The question paper will have ten questions
- Each full question consists of 16 marks.
- There will be 2 full questions (with a maximum of three subquestions) from each module.
- Each full question will have subquestions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Bernard Widrow and Samuel D. Stearns, "Adaptive Signal Processing", Person Education, 1985.

Reference Books:

1. Simon Haykin, "Adaptive Filter Theory", Pearson Education, 2003.
2. John R. Treichler, C. Richard Johnson, Michael G. Larimore, "Theory and Design of Adaptive Filters", Prentice-Hall of India, 2002.

ARTIFICIAL NEURAL NETWORKS

B.E., VI Semester, Electronics & Communication Engineering/ Telecommunication Engineering
[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC653	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (8 Hours /Module)	Exam Hours	03
CREDITS – 03			
<p>Course Objectives: The objectives of this course are:</p> <ul style="list-style-type: none"> • Understand the basics of ANN and comparison with Human brain • Provide knowledge on Generalization and function approximation and various architectures of building an ANN • Provide knowledge of reinforcement learning using neural networks • Provide knowledge of unsupervised learning using neural networks. 			
Module-1			RBT Level
<p>Introduction: Biological Neuron – Artificial Neural Model - Types of activation functions – Architecture :Feedforward and Feedback, Convex Sets, Convex Hull and Linear Separability, Non-Linear Separable Problem. XOR Problem, Multilayer Networks. Learning: Learning Algorithms, Error correction and Gradient Descent Rules, Learning objective of TLNs, Perceptron Learning Algorithm, Perceptron Convergence Theorem.</p>			L1, L2
Module-2			
<p>Supervised Learning: Perceptron learning and Non Separable sets, α-Least Mean Square Learning, MSE Error surface, Steepest Descent Search, μ-LMS approximate to gradient descent, Application of LMS to Noise Cancelling, Multi-layered Network Architecture, Backpropagation Learning Algorithm, Practical consideration of BP algorithm.</p>			L1, L2, L3
Module-3			
<p>Support Vector Machines and Radial Basis Function: Learning from Examples, Statistical Learning Theory, Support Vector Machines, SVM application to Image Classification, Radial Basis Function Regularization theory, Generalized RBF Networks, Learning in RBFNs, RBF application to face recognition.</p>			L1, L2, L3
Module-4			
<p>Attractor Neural Networks: Associative Learning Attractor Associative Memory, Linear Associative memory, Hopfield Network, application of Hopfield Network, Brain State in a Box neural Network, Simulated Annealing, Boltzmann Machine, Bidirectional Associative Memory.</p>			L1, L2, L3
Module-5			
<p>Self-organization Feature Map :Maximal Eigenvector Filtering, Extracting Principal Components, Generalized Learning Laws, Vector Quantization, Self-organization Feature Maps, Application of SOM, Growing Neural Gas.</p>			L1, L2, L3

Course outcomes: At the end of the course, students should be able to:

- Understand the role of neural networks in engineering, artificial intelligence, and cognitive modelling.
- Understand the concepts and techniques of neural networks through the study of the most important neural network models.
- Evaluate whether neural networks are appropriate to a particular application.
- Apply neural networks to particular applications, and to know what steps to take to improve performance.

Question paper pattern:

The question paper will have ten questions.

- Each full question consists of 16 marks.
- There will be 2 full questions (with a maximum of three subquestions) from each module.
- Each full question will have sub questions covering all the topics under a module. The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Neural Networks A Classroom Approach – Satish Kumar, McGraw Hill Education (India) Pvt. Ltd,
Second Edition.

Reference Books:

1. Introduction to Artificial Neural Systems- J.M. Zurada, Jaico Publications 1994.
2. Artificial Neural Networks- B. Yegnanarayana, PHI, New Delhi 1998.

DIGITAL SWITCHING SYSTEMS

B.E., VI Semester, Electronics & Communication Engineering/
Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC654	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (8 Hours /Module)	Exam Hours	03
CREDITS – 03			
<p>Course Objectives: This course will enable students to</p> <ul style="list-style-type: none"> • Understand the basics of telecommunication networks and digital transmission of data. • Study about the evolution of switching systems and the digital switching. • Study about the telecommunication traffic and its measurements. • Learn the technologies associated with the data switching operations. • Understand the use of software for the switching and its maintenance 			
Module-1			RBT Level
<p>DEVELOPMENT OF TELECOMMUNICATIONS: Network structure, Network services, terminology, Regulation, Standards. Introduction to telecommunication transmission, Power levels, Four wire circuits, Digital transmission, FDM, TDM, PDH and SDH [Text-1]</p>			L1, L2
Module-2			
<p>EVOLUTION OF SWITCHING SYSTEMS: Introduction, Message switching, Circuit switching, Functions of switching systems, Distribution systems, Basics of crossbar systems, Electronics switching. DIGITAL SWITCHING SYSTEMS: Switching system hierarchy, Evolution of digital switching systems, Stored program control switching systems, Building blocks of a digital switching system, Basic call processing. [Text-1 and 2]</p>			L1, L2
Module-3			
<p>TELECOMMUNICATIONS TRAFFIC: Introduction, Unit of traffic, Congestion, Traffic measurement, Mathematical model, lost call systems, Queuing systems. SWITCHING SYSTEMS: Introduction, Single stage networks, Gradings, Link Systems, GOS of Linked systems. [Text-1]</p>			L1, L2
Module-4			
<p>TIME DIVISION SWITCHING: Introduction, space and time switching, Time switching networks, Synchronisation. SWITCHING SYSTEM SOFTWARE: Introduction, Basic software architecture, Software architecture for level 1 to 3 control, Digital switching system software classification, Call models, Software linkages during call, Feature flow diagram, Feature interaction. [Text-1 and 2]</p>			L1, L2
Module-5			
<p>MAINTENANCE OF DIGITAL SWITCHING SYSTEM: Introduction, Software maintenance, Interface of a typical digital switching system central office, System outage and its impact on digital switching system reliability, Impact</p>			L1, L2

of software patches on digital switching system maintainability, A methodology for proper maintenance of digital switching system
A GENERIC DIGITAL SWITCHING SYSTEM MODEL: Introduction, Hardwarearchitecture,Softwarearchitecture,Recoverystrategy,Simplecall through a digital system, Common characteristics of digital switching systems. Reliability analysis.[Text-2]

Course Outcomes: At the end of the course, students should be able to:

- Identify the basic concepts and parameters of telecommunication networks and services.
- Identify the basic concepts and parameters of telecommunication networks and services.
- Model the traffic flow in lost call systems and queuing systems.
- Organize the digital switching software architecture for various levels of control.
- Identify the software aspects of switching systems and its maintenance.

Question paper pattern:

- The question paper will have ten questions
- Each full question consists of 16 marks.
- There will be 2 full questions (with a maximum of three subquestions) from each module.
- Each full question will have subquestions covering all the topics under a module
- The students will have to answer 5 full questions, selecting one full question from each module

Text Books:

1. Telecommunication and Switching, Traffic and Networks - JEFlood: Pearson Education, 2002.
2. Digital Switching Systems, Syed R. Ali, TMH Ed 2002.

Reference Book:

Digital Telephony - John C Bellamy: Wiley India Pvt. Ltd, 3rd Ed, 2008.

MICROELECTRONICS

B.E., VI Semester, Electronics & Communication Engineering/ Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC655	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of LectureHours	40 (8 Hours /Module)	Exam Hours	03
CREDITS – 03			
<p>Course Objectives: This course will enable students to:</p> <ul style="list-style-type: none"> • BefamiliarwiththeMOSFETphysicalstructureandoperation,terminal characteristics,circuitmodelsandbasiccircuitapplications. • Confrontintegrateddeviceand/orcircuitdesignproblems,identifythedesign issues, and developsolutions. • Analyzeanddesignmicroelectroniccircuitsforlinearamplifieranddigital applications. • Contrast the input/output and gain characteristics of single-transistor, differentialandcommontwo-transistorlinearamplifierbuildingblockstages. 			
Module-1			RBT Level
MOSFETS: Device Structure and Physical Operation, V-I Characteristics, MOSFET Circuits at DC, MOSFET as an amplifier and as a switch.			L1, L2
Module-2			
MOSFETS (continued): Biasing in MOS amplifier Circuits, Small Signal Operation and Models, Basic MOSFET amplifier, MOSFET internal capacitances, frequency response of CS amplifier.			L1, L2
Module-3			
MOSFETS (continued): Discrete circuit MOS amplifiers. Single Stage IC Amplifier: Comparison of MOSFET and BJT, Current sources, Current mirrors and Current steering circuits, high frequency response- general considerations.			L1, L2, L3
Module-4			
Single Stage IC Amplifier(continued) :CS with active loads, high frequency response of CS, CG amplifiers with active loads, high frequency response of CG, Cascode amplifiers. CS with source degeneration (only MOS amplifiers to be dealt).			L1, L2
Module-5			
Differential and Multistage Amplifiers: The MOS differential pair, small signal operation of MOS differential pair, Differential amplifier with active loads, and frequency response of the differential amplifiers. Multistage amplifiers (only MOS amplifiers to be dealt).			L1, L2
<p>Course outcomes: After studying this course, students will be ableto:</p> <ul style="list-style-type: none"> • Explain the underlying physics and principles of operation of Metaloxide-semiconductor(MOS)capacitorsandMOSfieldeffect transistors(MOSFETs). • DescribeandapplysimplelargesignalcircuitmodelsforMOSFETs. • Analyzeanddesignmicroelectroniccircuitsforlinearamplifierfordigitalapplications. 			

<ul style="list-style-type: none"> • Use of discrete MOS circuit to design single stage and multi stage amplifiers to meet stated operating specifications. 	
<p>Question paper pattern:</p> <ul style="list-style-type: none"> • The question paper will have ten questions • Each full question consists of 16 marks. • There will be 2 full questions (with a maximum of three subquestions) from each module. • Each full question will have subquestions covering all the topics under a module. • The students will have to answer 5 full questions, selecting one full question from each module. 	
<p>Text Book:</p> <p>“Microelectronic Circuits”, Adel Sedra and K.C. Smith, 6th Edition, Oxford University Press, International Version, 2009.</p>	
<p>Reference Books:</p> <ol style="list-style-type: none"> 1. “Microelectronics An integrated approach”, Roger T Howe, Charles G Sodini, Pearson education. 2. “Fundamentals of Microelectronics”, Behzad Razavi, John Wiley India Pvt. Ltd, 2008. 3. “Microelectronics – Analysis and Design”, Sundaram Natarajan, Tata McGraw- Hill, 2007. 	

EMBEDDED CONTROLLERLAB

B.E., VI Semester, Electronics & Communication Engineering/
Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15ECL67	IA Marks	20
Number of Lecture Hours/Week	01Hr Tutorial(Instructions) + 02 Hours Laboratory = 03	Exam Marks	80
RBT Levels	L1, L2, L3	Exam Hours	03
CREDITS – 02			
Course objectives: This course will enable students to: <ul style="list-style-type: none">• Understand the instruction set of ARM Cortex M3, a 32-bit microcontroller and the software tool required for programming in Assembly and C language.• Program ARM Cortex M3 using the various instructions in assembly level language for different applications.• Interface external devices and I/O with ARM Cortex M3.• Develop C language programs and library functions for embedded system applications.			
Laboratory Experiments			
PART-A: Conduct the following Study experiments to learn ALP using ARM Cortex M3 Registers using an Evaluation board and the required software tool. <ol style="list-style-type: none">1. ALP to multiply two 16 bit binary numbers.2. ALP to find the sum of first 10 integer numbers. PART-B: Conduct the following experiments on an ARM CORTEX M3 evaluation board using evaluation version of Embedded 'C' & Keil uVision-4 tool/compiler. <ol style="list-style-type: none">1. Display “Hello World” message using Internal UART.2. Interface and Control a DC Motor.3. Interface a Stepper motor and rotate it in clockwise and anti-clockwise direction.			

4. Interface a DAC and generate Triangular and Square waveforms.
5. Interface a 4x4 keyboard and display the key code on an LCD.
6. Using the Internal PWM module of ARM controller generate PWM and vary its duty cycle.
7. Demonstrate the use of an external interrupt to toggle an LED On/Off.
8. Display the Hex digits 0 to F on a 7-segment LED interface, with an appropriate delay in between.
9. Interface a simple Switch and display its status through Relay, Buzzer and LED.
10. Measure Ambient temperature using a sensor and SPI ADC IC.

Course outcomes: After studying this course, students will be able to:

- Apply the instruction set of 32 bit microcontroller ARM Cortex M3, and the software tool required for programming in Assembly and C language.
- Develop assembly language programs using ARM Cortex M3 for different applications
- Develop C language programs to interface external devices and I/O with ARM Cortex M3.
- Develop C language programs for embedded system applications.
- Develop C language programs which makes use of library functions for embedded system applications.

Conduction of Practical Examination:

1. PART-B experiments using Embedded-C are only to be considered for the practical examination. PART-A ALP programs are for study purpose and can be considered for Internal Marksevaluation.
2. Strictly follow the instructions as printed on the cover page of answerscript for breakup of marks.
3. Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

COMPUTER NETWORKS LABORATORY
 B.E., VI Semester, Electronics & Communication Engineering
 [As per Choice Based Credit System (CBCS) scheme]

Subject Code	15ECL68	IA Marks	20
Number of Lecture Hours/Week	01Hr Tutorial(Instructions) + 02 Hours Laboratory = 03	Exam Marks	80
RBT Levels	L1, L2, L3	Exam Hours	03

CREDITS – 02

Course objectives: This course will enable students to:

- Choosesuitabletoolstomodelanetworkandunderstandtheprotocolsatvarious OSI referencelevels.
- DesignasuitablenetworkandsimulateusingaNetworksimulator tool.
- SimulatethenetworkingconceptsandprotocolsusingC/C++programming.
- Modelthenetworksfordifferentconfigurationsandanalyzetheresults.

Laboratory Experiments

PART-A: Simulation experiments using NS2/ NS3/ OPNET/ NCTUNS/ NetSim/ QualNet or any other equivalent tool

1. Implement a point to point network with four nodes and duplex links between them. Analyze the network performance by setting the queue size and varying the bandwidth.
2. Implement a four node point to point network with links n0-n2, n1-n2 and n2-n3. Apply TCP agent between n0-n3 and UDP between n1-n3. Apply relevant application over TCP and UDP agents changing the parameter and determine the number of packets sent by TCP/UDP.
3. Implement Ethernet LAN using n(6-10) nodes. Compare the throughput by changing the error rate and data rate.
4. Implement Ethernet LAN using n nodes and assign multiple traffic to the nodes and obtain congestion window for different sources/destinations.
5. Implement ESS with transmission nodes in Wireless LAN and obtain the performance parameters.
6. Implementation of Link state routing algorithm.

PART-B: Implement the following in C/C++

1. Write a program for a HDLC frame to perform the following.
 - i) Bitstuffing
 - ii) Characterstuffing.
2. Write a program for distance vector algorithm to find suitable path for transmission.

3. Implement Dijkstra's algorithm to compute the shortest routing path.
4. For the given data, use CRC-CCITT polynomial to obtain CRC code. Verify the program for the cases
 - a. Without error
 - b. With error
5. Implementation of Stop and Wait Protocol and Sliding Window Protocol
6. Write a program for congestion control using leaky bucket algorithm.

Course outcomes: On the completion of this laboratory course, the students will be able to:

- Illustrate the operations of network protocols and algorithms using C programming.
- Utilize the network simulator for learning and practice of networking algorithms.
- Build the network with different configurations to measure the performance parameters.
- Develop the data link and routing protocols using C programming.
- Develop wired and wireless LAN protocol using network simulator

Conduct of Practical Examination:

- All laboratory experiments are to be included for practical examination.
- For examination one question from software and one question from hardware or only one hardware experiment based on the complexity to be set.
- Students are allowed to pick one experiment from the lot.
- Strictly follow the instructions as printed on the cover page of answers script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

6th Semester Open Electives Syllabus for the courses offered by EC/TC Board:

<p style="text-align: center;"><u>DATA STRUCTURE USING C++</u> B.E VI Semester (Open Elective) [As per Choice Based Credit System (CBCS) Scheme]</p>			
Course Code	15EC661	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (08 HrsperModule)	Exam Hours	03
CREDITS – 03			
Course objectives: This course will enable students to <ul style="list-style-type: none"> • Explainfundamentalsofdatastructuresandtheirapplicationsessentialfor programming/problemsolving • Analyze Linear Data Structures: Stack, Queues,Lists • Analyze Non Linear Data Structures:Trees • Assessappropriatedatastructureduringprogramdevelopment/ProblemSolving 			
Module -1			
INTRODUCTION:Functionsandparameters,Dynamicmemoryallocation,Recursion. LINEAR LISTS: Data objects and structures, Linear list data structures, Array Representation, Vector Representation, Singly Linked lists and chains. L1,L2			
Module -2			
ARRAYS AND MATRICES: Arrays, Matrices, Special matrices, Sparse matrices. STACKS:Theabstractdatatypes,ArrayRepresentation,LinkedRepresentation, Applications-Paranthesis Matching & Towers of Hanoi. L1, L2,L3			
Module -3			
QUEUES: The abstract data types, Array Representation, Linked Representation, Applications-Railroad car arrangement. HASHING: Dictionaries, Linear representation, Hash table representation. L1, L2, L3			
Module -4			
BINARYANDOTHERTREES:Trees,Binarytrees,Propertiesandrepresentationof binarytrees,Commonbinarytreeoperations,BinarytreetraversaltheADTbinary tree, ADT binary tree and the class linked binary tree. L1, L2,L3			
Module -5			
Priority Queues : Linear lists, Heaps, Applications-Heap Sorting. Search Trees:Binarysearchtreesoperationsandimplementation,BinarySearch trees with duplicates. L1, L2,L3			

Course outcomes: After studying this course, students will be able to:

- Acquire knowledge of Dynamic memory allocation, Various types of data structures, operations and algorithms and Sparse matrices and Hashing
- Understand non-Linear data structures trees and their applications
- Design appropriate data structures for solving computing problems
- Analyze the operations of Linear Data structures: Stack, Queue and Linked List and their applications

Text Book:

Data structures, Algorithms, and applications in C++, Sartaj Sahni, Universities Press, 2nd Edition, 2005.

Reference Books:

1. Data structures, Algorithms, and applications in C++, Sartaj Sahni, Mc. Graw Hill, 2000.
2. Object Oriented Programming with C++, E. Balaguruswamy, TMH, 6th Edition, 2013.
3. Programming in C++, E. Balaguruswamy. TMH, 4th, 2010.

POWER ELECTRONICS

B.E., VI Semester (Open Elective)
[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC662	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (08 Hours / Module)	Exam Hours	03
CREDITS – 03			
<p>Course Objectives: This course will enable students to</p> <ul style="list-style-type: none"> • Understand the working of various power devices. • Study and analysis of thyristor circuits with different triggering techniques. • Learn the applications of power devices in controlled rectifiers, converters and inverters. • Study of power electronics circuits under different load conditions. 			
Module-1			RBT Level
<p>Introduction - Applications of Power Electronics, Power Semiconductor Devices, Control Characteristics of Power Devices, types of Power Electronic Circuits. Power Transistors: Power BJTs: Steady state characteristics. Power MOSFETs: device operation, switching characteristics, IGBTs: device operation, output and transfer characteristics. (Text 1)</p>			L1, L2
Module-2			
<p>Thyristors - Introduction, Principle of Operation of SCR, Static Anode- Cathode Characteristics of SCR, Two transistor model of SCR, Gate Characteristics of SCR, Turn-ON Methods, Turn-OFF Mechanism, Turn-OFF Methods: Natural and Forced Commutation – Class A and Class B types, Gate Trigger Circuit: Resistance Firing Circuit, Resistance capacitance firing circuit. (Text 2)</p>			L1, L2, L3
Module-3			
<p>Controlled Rectifiers - Introduction, principle of phase controlled converter operation, Single phase full converters, Single phase dual converters. AC Voltage Controllers - Introduction, Principles of ON-OFF Control, Principle of Phase Control, Single phase control with resistive and inductive loads. (Text 1)</p>			L1, L2, L3
Module-4			
<p>DC-DC Converters - Introduction, principle of step-down operation and its analysis with RL load, principle of step-up operation, Step-up converter with resistive load, Performance parameters, Converter classification, Switching mode regulators: Buck regulator, Boost regulator, Buck-Boost Regulators. (Text 1)</p>			L1, L2

Module-5	
Pulse Width Modulated Inverters- Introduction, principle of operation, performance parameters, Single phase bridge inverters, voltage control of single phase inverters, current source inverters, Variable DC-link inverter, Boost inverter. <div style="text-align: right;">(Text1)</div>	L1, L2
Course outcomes: After studying this course, students will be able to: <ul style="list-style-type: none"> • Describe the characteristics of different power devices and identify the applications. • Illustrate the working of DC-DC converter and inverter circuit. • Determine the output response of a thyristor circuit with various triggering options. • Determine the response of controlled rectifier with resistive and inductive loads. 	
Evaluation of Internal Assessment Marks: It is suggested that at least a few experiments of Power Electronics are conducted by the students for better understanding of the course. This activity can be considered for the evaluation of 5 marks out of 20 Internal assessment marks, reserved for the other activities.	
Question paper pattern: <ul style="list-style-type: none"> • The question paper will have ten questions • Each full question consists of 16 marks. • There will be 2 full questions (with a maximum of three subquestions) from each module. • Each full question will have subquestions covering all the topics under a module • The students will have to answer 5 full questions, selecting one full question from each module 	
Text Book: <ol style="list-style-type: none"> 1. Mohammad H Rashid, Power Electronics, Circuits, Devices and Applications, 3rd/4th Edition, Pearson Education Inc, 2014, ISBN:978-93-325-1844-5. 2. M.D. Singh and K.B. Khanchandani, Power Electronics, 2nd Edition, Tata Mc-Graw Hill, 2009, ISBN:0070583897. 	
Reference Books: <ol style="list-style-type: none"> 4. L. Umanand, Power Electronics, Essentials and Applications, John Wiley India Pvt. Ltd, 2009. 5. Dr. P.S. Bimbhra, "Power Electronics", Khanna Publishers, Delhi, 2012. 6. P.C. Sen, "Modern Power Electronics", S Chand & Co New Delhi, 2005. 	

DIGITAL SYSTEM DESIGN USING VERILOG

B.E., VI Semester (Open Elective)
[As per Choice Based Credit System (CBCS) scheme]

Subject Code:	15EC663	IA Marks: 20
Number of Lecture Hours/Week:	03	Exam Marks: 80
Total Number of Lecture Hours:	40 (08 Hrs per module)	Exam Hours: 03
CREDITS – 03		
<p>Course objectives: This course will enable students to:</p> <ul style="list-style-type: none"> • Understand the concepts of Verilog Language. • Design the digital systems as an activity in a larger systems design context. • Study the design and operation of semiconductor memories frequently used in application specific digital system. • Inspect how effectively IC's are embedded in package and assembled in PCB's for different application. • Design and diagnosis of processors and I/O controllers used in embedded systems. 		
Module -1		RBT Level
<p>Introduction and Methodology: Digital Systems and Embedded Systems, Real-World Circuits, Models, Design Methodology (1.1, 1.3 to 1.5 of Text).</p> <p>Combinational Basics: Combinational Components and Circuits, Verification of Combinational Circuits. (2.3 and 2.4 of Text)</p> <p>Sequential Basics: Sequential Datapaths and Control Clocked Synchronous Timing Methodology (4.3 up to 4.3.1, 4.4 up to 4.4.1 of Text).</p>		L1, L2, L3
Module -2		
Memories: Concepts, Memory Types, Error Detection and Correction (Chap 5 of Text).		L1, L2, L3
Module -3		
Implementation Fabrics: Integrated Circuits, Programmable Logic Devices, Packaging and Circuit boards, Interconnection and Signal integrity (Chap 6 of Text).		L1, L2, L3
Module -4		
I/O interfacing: I/O devices, I/O controllers, Parallel Buses, Serial Transmission, I/O software (Chap 8 of Text).		L1, L2, L3
Module -5		
Design Methodology: Design flow, Design optimization, Design for test, Nontechnical Issues (Chap 10 of Text).		L1, L2, L3, L4
<p>Course outcomes: After studying this course, students will be able to:</p> <ul style="list-style-type: none"> • Apply the knowledge of digital fundamentals with combinational and Sequential circuits to design the Digital System • Identify different semiconductor memory used in application specific digital systems • Make use of the knowledge of embedded systems in small microcontrollers, larger CPUs/DSPs, or hard or soft processor cores. • Inspect different types of processor and I/O controllers that are used in embedded system. 		

- Develop Verilog model for sequential circuits and Inspect the test pattern generation.

Question paper pattern:

- The question paper will have ten questions.
- Each full question consisting of 16 marks. There will be 2 full questions (with a maximum of Three sub questions from each module).
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Peter J. Ashenden, "Digital Design: An Embedded Systems Approach Using VERILOG", Elsevier, 2010.

B.E E&CE EIGHTH SEMESTER SYLLABUS

Wireless Cellular and LTE 4G Broadband

B.E., VIII Semester, Electronics & Communication Engineering/ Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC81	IA Marks	20
Number of Lecture	04	Exam Marks	80
Total Number	50 (10 Hours / Module)	Exam Hours	03
CREDITS – 04			
<p>Course Objectives : This course will enable students to:</p> <ul style="list-style-type: none"> • Understand the basics of LTE standardization phases and specifications. • Explain the system architecture of LTE and E-UTRAN, the layer of LTE, based on the use of OFDMA and SC-FDMA principles. • Analyze the role of LTE radio interface protocols to setup, reconfigure and release the Radio Bearer, for transferring the EPS bearer. • Analyze the main factors affecting LTE performance including mobile speed and transmission bandwidth. 			
Module – 1			RBT Level
<p>Key Enablers for LTE features : OFDM, Single carrier FDMA, Single carrier FDE, Channel Dependent Multiuser Resource Scheduling, Multi antenna Techniques, IP based Flat network Architecture, LTE Network Architecture. (Sec 1.4- 1.5 of Text).</p> <p>Wireless Fundamentals: Cellular concept, Broadband wireless channel (BWC), Fading in BWC, Modeling BWC – Empirical and Statistical models, Mitigation of Narrowband and Broadband Fading (Sec 2.2 – 2.7 of Text).</p>			L1, L2
Module – 2			
<p>Multicarrier Modulation : OFDM basics, OFDM in LTE, Timing and Frequency Synchronization, PAR, SC-FDE (Sec 3.2 – 3.6 of Text).</p> <p>OFDMA and SC-FDMA: OFDM with FDMA, TDMA, CDMA, OFDMA, SC-FDMA, OFDMA and SC-FDMA in LTE (Sec 4.1 – 4.3, 4.5 of Text).</p> <p>Multiple Antenna Transmission and Reception: Spatial Diversity overview, Receive Diversity, Transmit Diversity, Interference cancellation and signal enhancement, Spatial Multiplexing, Choice between Diversity, Interference suppression and Spatial Multiplexing (Sec 5.1 – 5.6 of Text).</p>			L1, L2
Module – 3			
<p>Overview and Channel Structure of LTE : Introduction to LTE, Channel Structure of LTE, Downlink OFDMA Radio Resource, Uplink</p>			L1, L2

<p>SC-FDMA Radio Resource(Sec 6.1 – 6.4 of Text).</p> <p>Downlink Transport Channel Processing: Overview, Downlink shared channels, Downlink Control Channels, Broadcast channels, Multicast channels, Downlink physical channels, H-ARQ on Downlink(Sec 7.1 – 7.7 of Text).</p>	
Module – 4	
<p>Uplink Channel Transport Processing: Overview, Uplink shared channels, Uplink Control Information, Uplink Reference signals, Random Access Channels, H-ARQ on uplink (Sec 8.1 – 8.6 of Text).</p> <p>Physical Layer Procedures: Hybrid – ARQ procedures, Channel Quality Indicator CQI feedback, Precoder for closed loop MIMO Operations, Uplink channel sounding, Buffer status Reporting in uplink, Scheduling and Resource Allocation, Cell Search, Random Access Procedures, Power Control in uplink(Sec 9.1-9.6,9.8,9.9,9.10 Text).</p>	L1, L2
Module – 5	
<p>Radio Resource Management and Mobility Management : PDCP overview, MAC/RLC overview, RRC overview, Mobility Management, Inter-cell Interference Coordination(Sec 10.1 – 10.5 of Text).</p>	L1, L2
<p>Course Outcomes: At the end of the course, students will be able to:</p> <ul style="list-style-type: none"> • Make use of the system architecture and the functional standard specified in LTE 4G. • Identify the role of the layer of LTE radio interface protocols and EPS Data convergence protocols to set up, reconfigure and release data and voice from users. • Utilize the UTRAN and EPS handling processes from set up to release including mobility management for a variety of data call scenarios. • Identify the difference between uplink , down link and the physical layer procedures that provide the services to upper layers. • Utilize the Performance of resource management and packet data processing and transport algorithms. 	
<p>Question Paper pattern:</p> <ul style="list-style-type: none"> • The Question paper will have ten questions. • Each full Question consisting of 16 marks • There will be 2 full Questions (with a maximum of Three sub questions) from each module. • Each full question will have sub questions covering all the topics under a module. • The Students will have to answer 5 full Questions, selecting one full Question from each module. 	
<p>Text Book:</p> <p>Arunabha Ghosh, Jan Zhang, Jefferey Andrews, Riaz Mohammed, 'Fundamentals of LTE', Prentice Hall, Communications Engg. and Emerging Technologies.</p>	

Reference Books :

1. LTE for UMTS Evolution to LTE-Advanced' HarriHolma and AnttiToskala, Second Edition - 2011, John Wiley & Sons, Ltd. Print ISBN: 9780470660003.
2. 'EVOLVED PACKET SYSTEM (EPS) ; THE LTE AND SAE EVOLUTION OF 3G UMTS' by Pierre Lescuyer and Thierry Lucidarme, 2008, John Wiley & Sons, Ltd. PrintISBN:978-0-470-05976-0.
3. 'LTE – The UMTS Long Term Evolution ; From Theory to Practice' by StefaniaSesia,IssamToufik,andMatthewBaker,2009JohnWiley&Sons Ltd, ISBN978-0-470-69716-0.

Web Link and Video Lectures:

1. <https://www.coursera.org/courses?query=wireless>
2. <https://www.classcentral.com/course/wireless-communications-7503>

FIBER OPTICS and NETWORKS
 B.E., VIII Semester, Electronics & Communication Engineering
 [As per Choice Based Credit System (CBCS)]

Subject Code	15EC82	IA Marks	20
Number of Lecture Hours/Week	4	Exam Marks	80
Total Number of Lecture Hours	50(10 Hours / Module)	Exam Hours	03
CREDITS – 04			
<p>Course Objectives: This course will enable students to:</p> <ul style="list-style-type: none"> • Learn the basic principle of optical fiber communication with different modes of light propagation. • Understand the transmission characteristics and losses in optical fiber. • Study of optical components and its applications in optical communication networks. • Learn the network standards in optical fiber and understand the network architectures along with its functionalities. 			
Module -1			RBT Level
<p>Optical fiber Communications: Historical development, The general system, Advantages of optical fiber communication, Optical fiber waveguides: Ray theory transmission, Modes in planar guide, Phase and group velocity, Cylindrical fiber: Modes, Step index fibers, Graded index fibers, Single mode fibers, Cutoff wavelength, Mode field diameter, effective refractive index. Fiber Materials, Photonic crystal fibers. (Text 2)</p>			L1, L2
Module -2			
<p>Transmission characteristics of optical fiber: Attenuation, Material absorption losses, Linear scattering losses, Nonlinear scattering losses, Fiber bend loss, Dispersion, Chromatic dispersion, Intermodal dispersion: Multimode step index fiber.</p> <p>Optical Fiber Connectors: Fiber alignment and joint loss, Fiber splices, Fiber connectors, Fiber couplers. (Text 2)</p>			L1, L2
Module -3			
<p>Optical sources: Energy Bands, Direct and Indirect Bandgaps, Light Emitting diodes: LED Structures, Light Source Materials, Quantum Efficiency and LED Power, Modulation. Laser Diodes: Modes and Threshold conditions, Rate equation, External Quantum Efficiency, Resonant frequencies, Laser Diode structures and Radiation Patterns: Single mode lasers.</p> <p>Photodetectors: Physical principles of Photodiodes, Photodetector noise, Detector response time.</p> <p>Optical Receiver: Optical Receiver Operation: Error sources,</p>			L1, L2

Front End Amplifiers, Receiver sensitivity, Quantum Limit. (Text 1)	
Module -4	
WDM Concepts and Components: Overview of WDM: Operational Principles of WDM, WDM standards, Mach-Zehnder Interferometer Multiplexers, Isolators and Circulators, Fiber grating filters, Dielectric Thin-Film Filters, Diffraction Gratings, Active Optical Components, Tunable light sources, Optical amplifiers: Basic application and Types, Semiconductor optical amplifiers, Erbium Doped Fiber Amplifiers, Raman Amplifiers, Wideband Optical Amplifiers. (Text1)	L1, L2
Module -5	
Optical Networks: Optical network evolution and concepts: Optical networking terminology, Optical network node and switching elements, Wavelength division multiplexed networks, Public telecommunication network overview. Optical network transmission modes, layers and protocols: Synchronous networks, Asynchronous transfer mode, OSI reference model, Optical transport network, Internet protocol, Wavelength routing networks: Routing and wavelength assignment, Optical switching networks: Optical circuit switched networks, packet switched networks, Multiprotocol Label Switching, Optical burst switching networks, Optical network deployment: Long-haul networks, Metropolitan area networks, Access networks, Local area networks. (Text 2)	L1, L2
<p>Course Outcomes: At the end of the course, students will be able to:</p> <ul style="list-style-type: none"> • Classify and explain the working of optical fiber with different modes of signal propagation. • Utilize the concepts of transmission characteristics to obtain the losses in optical fiber communication. • Identify the construction and working principle of optical connectors, multiplexers and amplifiers. • Analyze the constructional features and the characteristics of optical sources and detectors. • Examine the networking aspects of optical fiber and describe various standards associated with it. 	
<p>Question Paper pattern:</p> <ul style="list-style-type: none"> • The Question paper will have ten questions. • Each full Question consisting of 16 marks • There will be 2 full Questions (with a maximum of Three sub questions) from each module. • Each full question will have sub questions covering all the topics under a module. • The Students will have to answer 5 full Questions, selecting one full Question from each module. 	
<p>Text Book s:</p> <ol style="list-style-type: none"> 1. Gerd Keiser , Optical Fiber Communication, 5th Edition, McGraw Hill 	

Education(India) Private Limited, 2015. ISBN:1-25-900687-5.

2. John M Senior, Optical Fiber Communications, Principles and Practice, 3rd Edition, Pearson Education, 2010, ISBN:978-81-317-3266-3

Reference Book :

JosephCPalais,FiberOpticCommunication,PearsonEducation,2005,
ISBN:0130085103

Web Link and Video Lectures:

1. <https://www.classcentral.com/tag/fiber-optics>
2. https://swayam.gov.in/nd1_noc20_ph07/preview

Micro Electro Mechanical Systems

B.E., VIII Semester, Electronics & Communication Engineering/ Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC831	IA Marks	20
Number of Lecture Hours/Week	03	Exam marks	80
Total Number of Lecture Hours	40 (8 Hours per Module)	Exam Hours	03
CREDITS – 03			
<p>Course Objectives: This course will enable students to:</p> <ul style="list-style-type: none"> • Understand overview of microsystems, their fabrication and application areas. • Working principles of several MEMS devices. • Develop mathematical and analytical models of MEMS devices. • Know methods to fabricate MEMS devices. • Various application areas where MEMS devices can be used. 			
Module 1			RBT Level
<p>Overview of MEMS and Microsystems: MEMS and Microsystem, Typical MEMS and Microsystems Products, Evolution of Microfabrication, Microsystems and Microelectronics, Multidisciplinary Nature of Microsystems, Miniaturization. Applications and Markets.</p>			L1, L2
Module 2			
<p>Working Principles of Microsystems: Introduction, Microsensors, Microactuation, MEMS with Microactuators, Microaccelerometers, Microfluidics.</p> <p>Engineering Science for Microsystems Design and Fabrication: Introduction, Molecular Theory of Matter and Inter-molecular Forces, Plasma Physics, Electrochemistry.</p>			L1, L2
Module 3			
<p>Engineering Mechanics for Microsystems Design: Introduction, Static Bending of Thin Plates, Mechanical Vibration, Thermomechanics, Fracture Mechanics, Thin Film Mechanics, Overview on Finite Element Stress Analysis.</p>			L1, L2, L3
Module 4			

Scaling Laws in Miniaturization: Introduction, Scaling in Geometry, Scaling in Rigid-Body Dynamics, Scaling in Electrostatic Forces, Scaling in Fluid Mechanics, Scaling in Heat Transfer.	L1,L2,L3
Module 5	
Overview of Micromanufacturing: Introduction, Bulk Micromanufacturing, Surface Micromachining, The LIGA Process, Summary on Micromanufacturing.	L1,L2
<p>Course Outcomes: After studying this course, students will be able to:</p> <ul style="list-style-type: none"> • Appreciate the technologies related to Micro Electro Mechanical Systems. • Understand design and fabrication processes involved with MEMS devices. • Analyse the MEMS devices and develop suitable mathematical models • Know various application areas for MEMS device 	
<p>Question paper pattern:</p> <ul style="list-style-type: none"> • The question paper will have 10 full questions carrying equal marks. • Each full question consists of 16 marks with a maximum of three sub questions. • There will be 2 full questions from each module covering all the topics of the module • The students will have to answer 5 full questions, selecting one full question from each module. 	
<p>Text Book:</p> <p>Tai-Ran Hsu, MEMS and Micro systems: Design, Manufacture and Nanoscale Engineering, 2nd Ed, Wiley.</p> <p>Reference Books:</p> <ol style="list-style-type: none"> 1. Hans H. Gatzert, Volker Saile, Jurg Leuthold, Micro and Nano Fabrication: Tools and Processes, Springer, 2015. 2. Dilip Kumar Bhattacharya, Brajesh Kumar Kaushik, Microelectromechanical Systems (MEMS), Cengage Learning. 	

SPEECH PROCESSING

B.E., VIII Semester, Electronics & Communication Engineering/ Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC832	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (8 Hours / Module)	Exam Hours	03
CREDITS – 03			
<p>Course Objectives: This course enables students to:</p> <ul style="list-style-type: none"> • Introduce the models for speech production • Develop time and frequency domain techniques for estimating speech parameters • Introduce a predictive technique for speech compression • Provide fundamental knowledge required to understand and analyse speech recognition, synthesis and speaker identification systems. 			
Modules			
Module-1			RBT Level
Fundamentals of Human Speech Production: The Process of Speech Production, Short-Time Fourier Representation of Speech, The Acoustic Theory of Speech Production, Lossless Tube Models of the Vocal Tract, Digital Models for Sampled Speech Signals			L1, L2
Module-2			
Time -Domain Methods for Speech Processing: Introduction to Short- Time Analysis of Speech, Short-Time Energy and Short-Time Magnitude, Short-Time Zero-Crossing Rate, The Short-Time Autocorrelation Function, The Modified Short-Time Autocorrelation Function, The Short-Time Average Magnitude Difference Function.			L1, L2
Module-3			
Frequency Domain Representations: Discrete-Time Fourier Analysis, Short-Time Fourier Analysis, Spectrographic Displays, Overlap Addition (OLA), Method of Synthesis, Filter Bank Summation (FBS) Method of Synthesis, Time-Decimated Filter Banks, Two-Channel Filter Banks, Implementation of the FBS Method Using the FFT, OLA Revisited, Modifications of the STFT.			L1, L2
Module-4			
The Cepstrum and Homomorphic Speech Processing: Homomorphic Systems for Convolution, Homomorphic Analysis of the Speech Model, Computing the Short-Time Cepstrum and Complex Cepstrum of Speech, Homomorphic Filtering of Natural Speech, Cepstrum Analysis of All-Pole Models, Cepstrum Distance Measures.			L1, L2, L3
Module-5			
Linear Predictive Analysis of Speech Signals: Basic Principles of Linear			L1, L2,

<p>Predictive Analysis, Computation of the Gain for the Model, Frequency Domain Interpretations of Linear Predictive Analysis, Solution of the LPC Equations, The Prediction Error Signal, Some Properties of the LPC Polynomial $A(z)$, Relation of Linear Predictive Analysis to Lossless Tube Models, Alternative Representations of the LP Parameters.</p>	<p>L3</p>
<p>Course outcomes: Upon completion of the course, students will be able to:</p> <ul style="list-style-type: none"> • Modelspeechproductionsystemanddescribethefundamentalsofspeech. • Extract and compare different speechparameters. • Choose an appropriate speech model for a givenapplication. • Analysespeechrecognition,synthesisandspeakeridentificationsystems 	
<p>Question paper pattern:</p> <ul style="list-style-type: none"> • The question paper will have tenquestions. • Each full question consists of 16marks. • Therewillbe2fullquestions(withamaximumofThreesubquestions)from eachmodule. • Each full question will have sub questions covering all the topics under a module.Thestudentswillhavetoanswer5fullquestions,selectingonefull question from eachmodule. 	
<p>Text Book :</p> <p style="padding-left: 40px;">Theory and Applications of Digital Speech Processing- Rabiner and Schafer, Pearson Education 2011</p>	
<p>Reference Books:</p> <ol style="list-style-type: none"> 3. Fundamentals of Speech Recognition- Lawrence Rabiner and Biing-Hwang Juang, Pearson Education,2003. 4. Speech and Language Processing–An Introduction to Natural Language Processing, Computational Linguistics, andSpeechRecognition- Daniel Jurafsky and James H Martin, Pearson Prentice Hall2009. 	

Radar Engineering B.E., VIII Semester, Electronics & Communication Engineering/ Telecommunication Engineering [As per Choice Based Credit System (CBCS) scheme]			
Subject Code	15EC833	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (8 Hours / Module)	Exam Hours	03
CREDITS – 03			
Course objectives: This course will enable students to: <ul style="list-style-type: none"> • Understand the Radar fundamentals and analyze the radar signals. • Understand various technologies involved in the design of radar transmitters and receivers. • Learn various radars like MTI, Doppler and tracking radars and their comparison 			
Modules			RBT Level
Module-1			
Basics of Radar: Introduction, Maximum Unambiguous Range, Radar Waveforms, Definitions with respect to pulse waveform-PRF, PRI, Duty Cycle, Peak Transmitter Power, Average transmitter Power. Simple form of the Radar Equation, Radar Block Diagram and Operation, Radar Frequencies, Applications of Radar, The Origins of Radar, Illustrative Problems. (Chapter 1 of Text)			L1, L2, L3
Module-2			
The Radar Equation: Prediction of Range Performance, Detection of signal in Noise, Minimum Detectable Signal, Receiver Noise, SNR, Modified Radar Range Equation, Envelope Detector — False Alarm Time and Probability, Probability of Detection, Radar Cross Section of Targets: simple targets – sphere, cone-sphere, Transmitter Power, PRF and Range Ambiguities, System Losses (qualitative treatment), Illustrative Problems. (Chapter 2 of Text, Except 2.4, 2.6, 2.8 & 2.11)			L1, L2, L3
Module-3			
MTI and Pulse Doppler Radar: Introduction, Principle, Doppler Frequency Shift, Simple CW Radar, Sweep to Sweep subtraction and Delay Line Canceler, MTI Radar with – Power Amplifier Transmitter, Delay Line Cancelers — Frequency Response of Single Delay- Line Canceler, Blind Speeds, Clutter Attenuation, MTI Improvement Factor, N- Pulse Delay-Line Canceler, Digital MTI Processing – Blind phases, I and Q Channels, Digital MTI Doppler signal processor, Moving Target Detector-Original MTD. (Chapter 3: 3.1, 3.2, 3.5, 3.6 of Text)			L1, L2, L3
Module-4			
Tracking Radar: Tracking with Radar-Types of Tracking Radar Systems, Monopulse Tracking- Amplitude Comparison Monopulse (one-and two-coordinates), Phase Comparison Monopulse. Sequential Lobing, Conical Scan Tracking, Block Diagram of Conical Scan			L1, L2, L3

Tracking Radar, Tracking in Range, Comparison of Trackers. (Chapter 4: 4.1, 4.2, 4.3 of Text)	
Module-5	
The Radar Antenna: Functions of The Radar Antenna, Antenna Parameters, Reflector Antennas and Electronically Steered Phased array Antennas. (Chapter 9: 9.1, 9.2 9.4, 9.5 ofText) Radar Receiver: The Radar Receiver, Receiver Noise Figure, Super HeterodyneReceiver, Duplexers and Receivers Protectors, Radar Displays. (Chapter 11 of Text)	L1, L2, L3
<p>Course outcomes: At the end of the course, students will be able to:</p> <ul style="list-style-type: none"> • Identify the fundamentals of radar ,tracking and antennas • Make use of the radar equation and process digital MTI with its applications • Utilize principle of doppler frequency shift and explain tracking radar antennas • Develop tracking radar and sequential lobbing • Analyze radar antenna parameters and tracking range 	
<p>Question paper pattern:</p> <ul style="list-style-type: none"> • The question paper will have ten questions. • Each full Question consisting of 16 marks • There will be 2 full questions (with a maximum of Three subquestions) from each module. • Each full question will have subquestions covering all the topics under a module. • The students will have to answer 5 full questions, selecting one full question from each module. 	
<p>Text Book: Introduction to Radar Systems- Merrill I Skolink, 3e, TMH, 2001.</p>	
<p>Reference Books:</p> <ol style="list-style-type: none"> 1. Radar Principles, Technology, Applications — Byron Edde, Pearson Education, 2004. 2. Radar Principles – Peebles. Jr, P.Z. Wiley. New York, 1998. 3. Principles of Modern Radar: Basic Principles – Mark A. Richards, James A. Scheer, William A. Holman. Yesdee, 2013 	

MACHINE LEARNING

B.E., VIII Semester, Electronics & Communication Engineering/ Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC834	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (8 Hours / Module)	Exam Hours	03
CREDITS – 03			
<p>Course Objectives: This course will enable students to:</p> <ul style="list-style-type: none"> • IntroducesomeconceptsandtechniquethatarecoretoMachineLearning. • Understand learning and decisiontrees. • Acquireknowledgeofneuralnetworks,Bayesianandinstantbased learning. • Understand analytical learning and reinforcedlearning. 			
Modules			
Module-1			RBT Level
Learning: Designing Learning systems, Perspectives and Issues, Concept Learning, Spaces and Candidate Elimination, Inductive bias.			Version Algorithm, L1, L2
Module-2			
Decision Tree and ANN: Decision Tree Representation, Hypothesis Space Search, Inductive bias in decision tree, issues in Decision tree. Neural Network Representation, Perceptrons, Multilayer Networks and Back Propagation Algorithms.			L1, L2
Module-3			
Bayesian and Computational Learning: Bayes Theorem, Bayes Theorem Concept Learning, Maximum Likelihood, Minimum Description Length Principle, Bayes Optimal Classifier, Gibbs Algorithm, Naïve Bayes Classifier.			L1, L2
Module-4			
Instant Based Learning and Learning set of rules: K- Nearest Neighbour Learning, Locally Weighted Regression, Radial Basis Functions, Case-Based Reasoning. Sequential Covering Algorithms, Learning Rule Sets, Learning First Order Rules, Learning Sets of First Order Rules.			L1, L2
Module-5			
Analytical Learning and Reinforced Learning: Perfect Domain Theories, Explanation Based Learning, Inductive-Analytical Approaches, Reinforcement Learning.			FOCL Algorithm, L1, L2
Course outcomes: At the end of the course, students should be able to:			

- Build the fundamental concepts of Machine learning.
- Make use of the underlying mathematical relationships within and across Machine Learning algorithms.
- Identify the paradigms of supervised and un-supervised learning.
- Develop a real world problem and apply the learned techniques of Machine Learning to solve the problem.
- Inspect Perfect Domain Theories, Inductive-Analytical Approaches and Reinforcement Learning.

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 16 marks.
- There will be 2 full questions (with a maximum of three subquestions) from each module.
- Each full question will have sub questions covering all the topics under a module. The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Machine Learning- Tom M. Mitchell, McGraw-Hill Education, (INDIAN EDITION), 2013.

Reference Books:

1. Introduction to Machine Learning- Ethem Alpaydin, 2nd Ed., PHI Learning Pvt. Ltd., 2013.
2. The Elements of Statistical Learning- T. Hastie, R. Tibshirani, J. H. Friedman, Springer; 1st edition, 2001.

NETWORK AND CYBER SECURITY

B.E., VIII Semester, Electronics & Communication Engineering

[As per Choice Based credit System (CBCS) Scheme

Subject Code	15EC835	IA Marks	20
Number of Lecture Hours/Week	03	Exam marks	80
Total Number of Lecture Hours	40 (8 Hours per Module)	Exam Hours	03
CREDITS – 03			
<p>Course Objectives: This course will enable students to:</p> <ul style="list-style-type: none"> • Know about security concerns in Email and Internet Protocol. • Understand cyber security concepts. • List the problems that can arise in cyber security. • Discuss the various cyber security framework. 			
Module-1			RBT Level
Transport Level Security: Web Security Considerations, Secure Sockets Layer, Transport Layer Security, HTTPS, Secure Shell (SSH) (Text 1: Chapter 15)			L1, L2
Module-2			
E-mail Security: Pretty Good Privacy, S/MIME, Domain keys identified mail (Text 1: Chapter 17)			L1, L2
Module-3			
IP Security: IP Security Overview, IP Security Policy, Encapsulation Security Payload (ESP), Combining security Associations Internet Key Exchange. Cryptographic Suites (Text 1: Chapter 18)			L1, L2
Module-4			
<p>Cyber network security concepts : Security Architecture, antipattern: signature based malware detection versus polymorphic threads, document driven certification and accreditation, policy driven security certifications. Refactored solution: reputational, behavioural and entropy based malware detection.</p> <p>The problems: cyber antipatterns concept, forces in cyber antipatterns, cyber anti pattern templates, cyber security antipattern catalog (Text-2: Chapter 1 & 2)</p>			L1, L2, L3
Module-5			
<p>Cyber network security concepts contd. : Enterprise security using Zachman framework Zachman framework for enterprise architecture, primitive models versus composite models, architectural problem solving patterns, enterprise workshop, matrix mining, mini patterns for problem solving meetings. Case study: cyber security hands on – managing administrations</p>			L1, L2, L3

<p>and root accounts, installing hardware, reimaging OS, installing system protection/antimalware, configuring firewalls (Text-2: Chapter 3 & 4).</p>	
<p>Course Outcomes: After studying this course, students will be able to:</p> <ul style="list-style-type: none"> • Explain network security protocols • Understand the basic concepts of cybersecurity • Discuss the cyber security problems • Explain Enterprise Security Framework • Apply concept of cybersecurity framework in computer system administration 	
<p>Question paper pattern:</p> <ul style="list-style-type: none"> • The question paper will have 10 full questions carrying equal marks. • Each full question consists of 16 marks with a maximum of Three sub questions. • There will be 2 full questions from each module covering all the topics of the module • The students will have to answer 5 full questions, selecting one full question from each module. 	
<p>Text Books :</p> <ol style="list-style-type: none"> 1. William Stallings, “Cryptography and Network Security Principles and Practice”, Pearson Education Inc., 6th Edition, 2014, ISBN: 978-93-325- 1877-3. 2. Thomas J. Mowbray, “Cyber Security – Managing Systems, Conducting Testing, and Investigating Intrusions”, Wiley. 	
<p>Reference Books :</p> <ol style="list-style-type: none"> 1. Cryptography and Network Security, Behrouz A. Forouzan, TMH, 2007. 2. Cryptography and Network Security, Atul Kahate, TMH, 2003. 	