K.S.INSTITUTE OF TECHNOLOGY, BANGALORE

(AFFLIATED TO VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELGAUM)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGG.

ENGINEERING MATHEMATICS-III
(Common to all Branches)

Course Title: Engineering Mathematics-III | **Course Code : 15MAT31**
Credits:04 | **L-T-P :4-0-0**
Contact Hours/Week: 04 | **Total Hours:50**
Exam. Marks:80 | **IA Marks :20**
Exam. Hours : 03

Course Learning Objectives:

- TohaveaninsightintoFourierseries,Fouriertransforms,Laplacetransforms,Difference equations andZ-transforms.
- To develop the proficiency in variational calculus and solving ODE's arising in engineering applications, using numericalmethods.

Module-1

Laplace Transforms: Definition and Laplace transform of elementary functions. Laplace transforms of Periodic functions and unit-step function – problems.
Inverse Laplace Transforms: Inverse Laplace transform - problems, Convolution theorem to find the inverse Laplace transform (without proof) and problems, solution of linear differential equations using Laplace transform.

Module-2

Fourier Series: Periodic functions, Dirichlet's condition. Fourier series of periodic functions period 2n and arbitrary period. Half range Fourier series. Practical harmonic analysis, examples from engineering field.

Module-3

Fourier Transforms: Infinite Fourier transforms, Fourier sine and cosine transforms. Inverse Fourier transforms. Simple problems.
Difference Equations and Z-Transforms: Difference equations, basic definition, z-transform-definition, Standard z-transforms, Damping and shifting rules, initial value and final value theorems (without proof) and problems, Inverse z-transform. Simple problems.

Module-4

Numerical Solutions of Ordinary Differential Equations (ODE's): Numerical solution of ODE's of first order and first degree- Taylor's series method, Modified Euler's method. Range - Kutta method of fourth order, Milne's and Adam-Bashforth predictor and corrector method (No derivations of formulae), Problems.

Module-5

Numerical Solution of Second Order ODE's: Runge -Kutta method and Milne's predictor and corrector method.(No derivations of formulae).
Calculus of Variations: Variation of function and functional, variational problems, Euler's equation, Geodesics, hanging chain, problems.

Course Outcomes: At the end of the course the student will be able to:

- CO1: Use Laplace transform and inverse Laplace transform in solving differential/ integral equation arising in network analysis, control systems and other fields ofengineering.
- CO2: Demonstrate Fourier series to study the behaviour of periodic functions and their applications in system communications, digital signal processing and fieldtheory.
- CO3: Make use of Fourier transform and Z-transform to illustrate discrete/continuous function arising in wave and heat propagation, signals andsystems.
- CO4: Solve first and second order ordinary differential equations arising in engineering problems using single step and multistep numericalmethods.
- CO5:Determine the extremals of functionals using calculus of variations and solve problems arising in dynamics of rigid bodies and vibrationalanalysis.

Question paper pattern:

1. The question paper will have ten full questions carrying equalmarks.
2. Each full question will be for 20marks.

- Therewillbetwofullquestions(withamaximumoffoursub-questions)fromeachmodule.

Sl. No.	Title of the Book	Name of the Author/s	Name of the Publisher	Edition and Year
Textbooks				
1	Advanced Engineering Mathematics	E. Kreyszig	John Wiley & Sons	10th Edition, 2016
2	Higher Engineering Mathematics	B. S. Grewal	Khanna Publishers	44th Edition, 2017
3	Engineering Mathematics	Srimanta Pal et al	Oxford University Press	3rd Edition, 2016
Reference Books				
1	Advanced Engineering Mathematics	C. Ray Wylie, Louis C. Barrett	McGraw-Hill Book Co	6th Edition, 1995
2	Introductory Methods of Numerical Analysis	S. S. Sastry	Prentice Hall of India	4th Edition 2010
3	Higher Engineering Mathematics	B.V. Ramana	McGraw-Hill	11th Edition,2010
4	A Text Book of Engineering Mathematics	N. P. Baliand ManishGoyal	Laxmi Publications	2014
5	Advanced Engineering Mathematics	Chandrika Prasad and Reena Garg	Khanna Publishing,	2018

Web links and Video Lectures:

1. http://nptel.ac.in/courses.php?disciplineID=111
2. http://www.class-central.com/subject/math(MOOCs)
3. http://academicearth.org/
4. VTU EDUSAT PROGRAMME -20

B. E. (EC / TC)
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
SEMESTER – III
NETWORK THEORY

Course Code	**18EC32**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03 + 2 (Tutorial)**	**SEE marks**	**60**
		Exam Hours	**03**

CREDITS – 04

Course Learning Objectives: This course will enable students to:

- Analyze ac and dc electrical networks.
- Simplify electrical circuits using network theorems.
- Apply transient behavior and initial conditions to find response of RLC circuits.
- Apply Laplace transforms and transient analysis to find response of RLC circuits.
- Determine the various parameters of Series and Parallel resonance circuits and analyze two port network parameters.

Modules	RBT Level
Module –1	
Basic Concepts: Practical sources, Source transformations, Network reduction using Star – Delta transformation, Loop and node analysis with linearly dependent and independent sources for DC and AC networks.	**L1, L2, L3, L4**
Module –2	
Network Theorems: Superposition, Millman's theorems, Thevinin's and Norton's theorems, Maximum Power transfer theorem.	**L1, L2, L3, L4**
Module –3	
Transient behavior and initial conditions: Behavior of circuit elements under switching condition and their Representation, evaluation of initial and final conditions in RL, RC and RLC circuits for AC and DC excitations.	**L1 , L2 , L3**
Module –4	
Laplace Transformation & Applications: Solution of networks, step, ramp and impulse responses, waveform Synthesis.	**L1, L2, L3, L4**
Module –5	
Two port network parameters: Definition of Z, Y, h and Transmission parameters, modelling with these parameters, relationship between parameters sets. **Resonance:** **Series Resonance**: Variation of Current and Voltage with Frequency, Selectivity and Bandwidth, Q-Factor, Circuit Magnification Factor, Selectivith with Variable Capacitance, Selectivity with Variable Inductance. **Parallel Resonance:** Selectivity and Bandwidth, Maximum Impedance Conditions with C, L and f Variable, current in Anti-Resonant Circuit, The General Case-Resistance Present in both Branches.	**L1, L2, L3, L4**

Course Outcomes: At the end of the course, the students will be ableto

- Analyze ac and dc electrical networks.
- Simplify electrical circuits using network theorems.
- Apply transient behavior and initial conditions to find response of RLC circuits.
- Apply Laplace transforms and transient analysis to find response of RLC circuits.
- Determine the various parameters of Series and Parallel resonance circuits and analyze two port network parameters.

Question paper pattern:

□ Examinationwillbeconductedfor100markswithquestionpapercontaining10fullquestions,eachof20marks.
□ Each full question can have a maximum of 4 subquestions.
□ Therewillbe2fullquestionsfromeach modulecoveringallthetopicsofthemodule.
□ Studentswillhavetoanswer5 fullquestions,selectingonefullquestionfromeachmodule.
□ The total marks will be proportionally reduced to 60 marks as SEE marks is60.

Text Books:

1. M.E.VanValkenberg(2000),—Networkanalysis|,PrenticeHallofIndia,3rdedition,2000,ISBN:9780136110958.
2. RoyChoudhury,—Networksandsystems|,2ndedition,NewAgeInternationalPublications,2006,ISBN: 9788122427677

Reference Books:

1. Hayt,KemmerlyandDurbin—EngineeringCircuitAnalysis|,TMH7thEdition,2010.
2. J.DavidIrwin/R.MarkNelms,—BasicEngineeringCircuitAnalysis|,JohnWiley,8thed,2006.
3. CharlesKAlexanderandMathewNOSadiku,—FundamentalsofElectricCircuits|,TataMcGraw-Hill,3rdEd,2009.

Web links and Video Lectures:

1. https://www.classcentral.com/course/edx-circuits-and-electronics-1-basic-circuit-analysis-444
2. https://nptel.ac.in/courses/108/105/108105159/

B. E. (EC / TC)
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
SEMESTER – III
ELECTRONIC DEVICES

Course Code	**18EC33**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE marks**	**60**
Total Number of Lecture Hours	**40 (8 Hours / Module)**	**Exam Hours**	**03**

CREDITS – 03

Course Learning Objectives: This course will enable students to:
□ Understand the basics of semiconductor physics and electronicdevices.
□ Describe the mathematical models BJTs and FETs along with the constructionaldetails.
□ Understand the construction and working principles of optoelectronicdevices
□ Understandthefabricationprocessofsemiconductordevicesand CMOSprocessintegration.

Module-1	RBT Level
Semiconductors Bondingforcesinsolids,Energybands,Metals,SemiconductorsandInsulators,Direct and Indirect semiconductors, Electrons and Holes, Intrinsic and Extrinsic materials, ConductivityandMobility,DriftandResistance,Effectsoftemperatureanddopingon mobility,HallEffect.**(Text1:3.1.1,3.1.2,3.1.3,3.1.4,3.2.1,3.2.3,3.2.4,3.4.1,3.4.2, 3.4.3, 3.4.5).**	**L1,L2**
Module-2	
P-N Junctions ForwardandReversebiasedjunctions-QualitativedescriptionofCurrentflowata junction, reverse bias, Reverse bias breakdown- Zener breakdown, avalanche breakdown,Rectifiers.**(Text1:5.3.1,5.3.3,5.4,5.4.1,5.4.2,5.4.3)** OptoelectronicDevicesPhotodiodes:CurrentandVoltageinanIlluminatedJunction, SolarCells,Photodetectors.LightEmittingDiode:LightEmittingmaterials.**(Text1: 8.1.1, 8.1.2, 8.1.3, 8.2, 8.2.1)**	**L1,L2**
Module – 3	
Bipolar Junction Transistor Fundamentals of BJT operation, Amplification with BJTS, BJT Fabrication, The coupledDiodemodel(Ebers-MollModel),Switchingoperationofatransistor,Cutoff, saturation,switchingcycle,specifications,Driftinthebaseregion,Basenarrowing, Avalanche breakdown. **(Text 1: 7.1, 7.2, 7.3, 7.5.1, 7.6, 7.7.1, 7.7.2, 7.7.3).**	**L1,L2**
Module-4	
Field Effect Transistors Basic pn JFET Operation, Equivalent Circuit and Frequency Limitations, MOSFET- Two terminal MOS structure- Energy band diagram, Ideal Capacitance – Voltage CharacteristicsandFrequencyEffects,BasicMOSFETOperation-MOSFETstructure, Current-VoltageCharacteristics.**(Text2:9.1.1,9.4,9.6.1,9.6.2,9.7.1,9.7.2,9.8.1, 9.8.2).**	**L1,L2**
Module-5	
Fabrication of p-n junctions ThermalOxidation,Diffusion,RapidThermalProcessing,Ionimplantation,chemical vapour deposition, photolithography, Etching, metallization. **(Text 1: 5.1)** **IntegratedCircuits** Background, Evolution of ICs, CMOS Process Integration, Integration of Other Circuit Elements. **(Text 1: 9.1, 9.2, 9.3.1, 9.3.3).**	**L1,L2**

Course outcomes: After studying this course, students will be able to:

- Apply the principles of semiconductor physics to electronic devices.
- Identify the characteristics of semiconductor and Optoelectronic devices.
- Analyze the BJTs and FETs circuits using mathematical model.
- Identify the operation of FET and its frequency limitation.
- Identify the fabrication process of semiconductor devices and CMOS process integration.

Question paper pattern:

□ Examinationwillbeconductedfor100markswithquestionpapercontaining10fullquestions,eachof20marks.
□ Each full question can have a maximum of 4 subquestions.
□ Therewillbe2fullquestionsfromeach modulecoveringallthetopicsofthemodule.
□ Studentswillhavetoanswer5fullquestions,selectingonefullquestionfromeachmodule.
□ Thetotalmarkswillbeproportionallyreduced to60marksas SEEmarksis60.

Text Books:

1. Ben.G.Streetman,SanjayKumarBanergee,"SolidStateElectronicDevices",7thEdition,PearsonEducation, 2016, ISBN978-93-325-5508-2.
2. DonaldANeamen,DhrubesBiswas,"SemiconductorPhysicsandDevices",4thEdition,MCGrawHill Education, 2012, ISBN978-0-07-107010-2.

Reference Book:

1. S.M.Sze,KwokK.Ng,"PhysicsofSemiconductorDevices",3rdEdition,Wiley,2018.
2. A. Bar-Lev, "Semiconductor and Electronic Devices", 3rd Edition, PHI,1993.

Web links and Video Lectures:

1. https://nptel.ac.in/courses/117/106/117106091/
2. https://www.edx.org/course/electronic-materials-and-devices

B. E. (EC / TC)
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
SEMESTER – III

DIGITAL SYSTEM DESIGN

Course Code	**18EC34**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SIE Marks**	**60**
Total Number of Lecture Hours	**40 (08 Hours per Module)**	**Exam Hour**	**03**

CREDITS – 03

Course Learning Objectives: This course will enable students to:

- IllustratesimplificationofAlgebraicequationsusingKarnaughMapsandQuine-McCluskyTechniques.
- DesignDecoders,Encoders,DigitalMultiplexer,Adders,SubtractorsandBinaryComparators.
- Describe Latches and Flip-flops, Registers andCounters.
- Analyze Mealy and MooreModels.
- Develop state diagrams Synchronous SequentialCircuits.
- Appreciate the applications of digitalcircuits.

Module – 1	**RBT Level**
Principles of combinational logic: Definition of combinational logic, canonical forms, Generation of switching equations from truth tables, Karnaugh maps-3,4,5 variables, Incompletely specified functions (Don‘t care terms) Simplifying Max term equations, Quine-McClusky techniques – 3 & 4 variables. **(Text 1 - Chapter 3)**	**L1, L2, L3**
Module – 2	
Analysis and design of combinational logic: Decoders, Encoders, Digital multiplexers, Adders and subtractors, Look ahead carry, Binary comparators.**(Text 1 - Chapter 4).** Programmable Logic Devices, Complex PLD, FPGA. **(Text 3 - Chapter 9, 9.6 to 9.8)**	**L1, L2, L3**
Module -3	
Flip-Flops and its Applications: Basic Bistable elements, Latches, The master-slave flip-flops (pulse-triggered flip-flops): SR flip-flops, JK flip-flops, Characteristic equations, Registers, binary ripple counters, and synchronous binary counters.**(Text 2 - Chapter 6)**	**L1, L2, L3**
Module -4	
Sequential Circuit Design: Design of a synchronous counter,Design of a synchronous mod-n counter using clockedJK, D, T and SR flip-flops. **(Text 2 - Chapter 6)** Mealy and Moore models, State machine notation, Construction of state diagrams.**(Text 1 - Chapter 6)**	**L1, L2, L3**
Module -5	
Applications of Digital Circuits: Design of a Sequence Detector, Guidelines for construction of state graphs, Design Example – Code Converter, Design of Iterative Circuits (Comparator), Design of Sequential Circuits using ROMs and PLAs,CPLDs and FPGAs, Serial Adder with Accumulator, Design of Binary Multiplier, Design of Binary Divider. **(Text 3 – 14.1, 14.3, 16.2, 16.3, 16.4, 18.1, 18.2, 18.3)**	**L1, L2, L3**

Course Outcomes: After studying this course, students will be able to:

- Simplify switching equations using K-map and Quine Mc-Cluskey techniques.
- Design combinational logic circuits.
- Design sequential logic circuits.
- Analyze sequential logic circuits using Mealy and Moore Finite state machine
- Design complex digital circuits for various applications.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20marks.
- Each full question can have a maximum of 4 subquestions.
- Therewillbe2fullquestionsfromeachmodulecoveringallthetopicsofthemodule.

- Studentswillhavetoanswer5fullquestions,selectingonefullquestionfromeachmodule.
- Thetotalmarkswillbeproportionallyreduced to60 marksasSEEmarksis60.

Text Books:

1. John M Yarbrough,-Digital Logic Applications and Design, ThomsonLearning,2001.
2. DonaldD.Givone,—DigitalPrinciplesandDesign|,McGrawHill,2002.
3. CharlesHRothJr.,LarryL.Kinney—FundamentalsofLogicDesign,CengageLearning,7th Edition.

Reference Books:

1. D.P.KothariandJ.SDhillon,—DigitalCircuitsandDesign|,Pearson,2016,
2. MorrisMano,—DigitalDesign|,PrenticeHallofIndia,ThirdEdition.
3. K.A.Navas,—ElectronicsLabManual|,VolumeI,PHI,5thEdition,2015.

Web links and Video Lectures:

1. https://www.classcentral.com/course/swayam-digital-electronic-circuits-12953
2. https://nptel.ac.in/courses/117/106/117106086/

B. E. (EC / TC)
ChoiceBasedCreditSystem(CBCS)andOutcomeBasedEducation(OBE) SEMESTER – III

COMPUTER ORGANIZATION AND ARCHITECTURE

Course Code	**18EC35**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (08Hours per Module)**	**Exam Hours**	**03**

CREDITS– 03

Course Learning Objectives: This course will enable students to:

- Explainthebasicsubsystemsofacomputer,theirorganization,structureandoperation.
- Illustrate the concept of programs as sequences of machineinstructions.
- Demonstrate different ways of communicating with I/Odevices
- Describe memory hierarchy and concept of virtualmemory.
- Illustrate organization of simple pipelined processor and other computingsystems.

Module 1	**RBT Level**
Basic Structure of Computers: Computer Types, Functional Units, Basic Operational Concepts, Bus Structures, Software, Performance – Processor Clock, Basic Performance Equation **(upto 1.6.2 of Chap 1 of Text).** **Machine Instructions and Programs:** Numbers, Arithmetic Operations and Characters, IEEE standard for Floating point Numbers, Memory Location and Addresses, Memory Operations, Instructions and Instruction Sequencing **(upto 2.4.6 of Chap 2 and 6.7.1 of Chap 6 of Text).**	**L1, L2, L3**
Module2	
Addressing Modes, Assembly Language, Basic Input and Output Operations, Stacks and Queues, Subroutines, Additional Instructions **(from 2.4.7 of Chap 2, except 2.9.3, 2.11 & 2.12 of Text).**	**L1, L2, L3**
Module3	
Input/Output Organization: Accessing I/O Devices, Interrupts – Interrupt Hardware, EnablingandDisablingInterrupts,HandlingMultipleDevices,ControllingDeviceRequests, DirectMemoryAccess**(upto4.2.4and4.4except4.4.1ofChap4ofText).**	**L1, L2, L3**
Module4	
Memory System: Basic Concepts, Semiconductor RAM Memories-Internal organization of memory chips, Static memories, Asynchronous DRAMS, Read Only Memories, Cash Memories,VirtualMemories,SecondaryStorage-MagneticHardDisks**(5.1,5.2,5.2.1,5.2.2, 5.2.3, 5.3, 5.5 (except 5.5.1 to 5.5.4), 5.7 (except 5.7.1), 5.9, 5.9.1 of Chap 5 of Text).**	**L1, L2, L3**
Module5	
Basic Processing Unit: Some Fundamental Concepts, Execution of a Complete Instruction, Multiple Bus Organization, Hardwired Control, Microprogrammed Control **(upto 7.5 except 7.5.1 to 7.5.6 of Chap 7 of Text).**	**L1,L2, L3**

Course Outcomes: After studying this course, students will be able to:

- Categorize the operations of major subsystems of computer
- Analyze different types of semiconductor memories and secondary memories.
- Analyze ALU and control unit operations.
- Analyze the working of stacks, queues, subroutines and handling different types of interrupts.
- Apply the concepts of hardwired control and microprogrammed control.

Question paper pattern:

- Examinationwillbeconductedfor100markswithquestionpapercontaining10fullquestions,eachof 20marks.
- Each full question can have a maximum of 4 subquestions.
- Therewillbe2fullquestionsfromeachmodulecoveringallthetopicsofthemodule.
- Studentswillhavetoanswer5fullquestions,selectingonefullquestionfromeachmodule
- Thetotalmarkswillbeproportionallyreduced to60 marksasSEEmarksis60.

Text Book:

1. Carl Hamacher, ZvonkoVranesic, SafwatZaky: Computer Organization, 5th Edition, Tata McGraw Hill, 2002.

Reference Books:

1. David A. Patterson, John L. Hennessy: Computer Organization and Design – The Hardware / Software Interface ARM Edition, 4th Edition, Elsevier,2009.
2. WilliamStallings:ComputerOrganization&Architecture,7thEdition,PHI,2006.
3. VincentP.Heuring&HarryF.Jordan:ComputerSystemsDesignandArchitecture,2ndEdition,Pearson Education,2004.

Web links and Video Lectures:

1. https://www.classcentral.com/course/swayam-computer-organization-and-architecture-a-pedagogical-aspect-9824
2. https://online-learning.harvard.edu/course/computer-architecture-0

B. E. (EC / TC) ChoiceBasedCreditSystem(CBCS)andOutcomeBasedEducation(OBE) SEMESTER – III			
POWER ELECTRONICS AND INSTRUMENTATION			
Course Code	**18EC36**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of LectureHours	**40 (8 Hours/ Module)**	**Exam Hours**	**03**
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Study and analysis of thyristor circuits with different triggeringconditions.
- Learntheapplicationsofpowerdevices incontrolledrectifiers,convertersandinverters.
- Understand types of instrumenterrors.
- Develop circuits for multirange Ammeters andVoltmeters.
- Describe principle of operation of digital measuring instruments andBridges.
- Understand the operation of Transducers, Instrumentation amplifiers andPLCs.

Module-1	RBT Level
Introduction: History, Power Electronic Systems, Power Electronic Converters and Applications (**1.2, 1.3 1.5 & 1.6 of Text 1).** **Thyristors:** Static Anode-Cathode characteristics and Gate characteristics of SCR, Turn-ON methods, Turn-OFFmechanisms(**2.3, 2.6 without 2.6.1), 2.7, 2.9 of text 1**), Turn-OFF Methods: Natural and Forced Commutation – Class A and Class B types (**refer 2.10 without design considerations**), Gate Trigger Circuit: Resistance Firing Circuit, Resistance capacitance firing circuit (**refer 3.5 upto 3.5.2 of Text 1**), Unijunction Transistor: Basic operation and UJT Firing Circuit (**refer 3.6, upto 3.6.4, except 3.6.2**).	**L1, L2**
Module-2	
Phase Controlled Converter: Control techniques, Single phase half wave and full wave controlled rectifier with resistive and inductive loads, effect of freewheeling diode (**refer Chapter 6 of Text 1 upto6.4.1 without derivations**). **Choppers:** Chopper Classification, Basic Chopper operation: step-down, step-up and step-up/down choppers. (**refer Chapter 8 of Text 1upto 8.3.3**)	**L1,L2, L3**
Module-3	
Inverters: Classification, Single phase Half bridge and full bridge inverters with R and RL load (**refer Chapter 9 of Text 1 upto 9.4.2 without CircuitAnalysis**). **Switched Mode Power Supplies**: Isolated Flyback Converter, Isolated Forward Converter(**only refer to the circuit operations in section 16.3 of Text 1upto 16.3.2 except 16.3.1.3 and derivations**). **Principles of Measurement:** Static Characteristics, Error in Measurement, Types of Static Error. (Text 2:1.2-1.6) Multirange Ammeters, Multirange voltmeter. (Text 2: 3.2, 4.4)	**L1,L2, L3**
Module-4	

Digital Voltmeter: Ramp Technique, Dual slope integrating Type DVM, Direct Compensation type and Successive Approximations type DVM (Text 2: 5.1-5.3, 5.5, 5.6) **DigitalMultimeter:**DigitalFrequencyMeterandDigitalMeasurementofTime,Function Generator. **Bridges:**Measurementofresistance:Wheatstone'sBridge,ACBridges-Capacitanceand Inductance Comparison bridge, Wien'sbridge. (Text 2: refer 6.2, 6.3 upto 6.3.2, 6.4 upto 6.4.2, 8.8, 11.2, 11.8-11.10, 11.14).	**L1, L2**
Module-5	
Transducers: Introduction,ElectricalTransducer,ResistiveTransducer,Resistive position Transducer, Resistance Wire Strain Gauges, Resistance Thermometer, Thermistor,LVDT. (Text 2: 13.1-13.3, 13.5, 13.6 upto 13.6.1, 13.7, 13.8, 13.11). InstrumentationAmplifierusingTransducerBridge,Temperatureindicatorsusing Thermometer,AnalogWeightScale(Text2:14.3.3,14.4.1,14.4.3). **Programmable Logic Controller:** Structure, Operation, Relays and Registers (Text 2: 21.15, 21.15.2, 21.15.3, 21.15.5, 21.15.6).	**L1,L2, L3**

Course Outcomes: At the end of the course students should be able to:

- Analyse the SCR characteristics, turn-on and turn-off mechanisms.
- Analyse the power electronic converters and controllers.
- Identify the measurement errors and characteristics of the instruments.
- Determine the unknown value of AC Bridges.
- Analyse operations of digital measuring instruments, Transducers and PLCs.

Question paper pattern:

- Examinationwillbeconductedfor100markswithquestionpapercontaining10fullquestions,eachof 20marks.
- Each full question can have a maximum of 4 subquestions.
- Therewillbe2fullquestionsfromeachmodulecoveringallthetopicsofthemodule.
- Studentswillhavetoanswer5fullquestions,selectingonefullquestionfromeachmodule.
- Thetotalmarkswillbeproportionallyreduced to60 marksasSEEmarksis60.

Text Books:

1. M.D Singh and K B Khanchandani, Power Electronics, 2nd Edition, Tata Mc-Graw Hill, 2009, ISBN: 0070583897
2. H.S.Kalsi,"ElectronicInstrumentation",McGrawHill,3rd Edition, 2012, ISBN:9780070702066.

Reference Books:

1. Mohammad H Rashid, Power Electronics, Circuits, Devices and Applications, 3rd/4th Edition, Pearson Education Inc, 2014, ISBN:978-93-325-1844-5.
2. L.Umanand,PowerElectronics,EssentialsandApplications,JohnWileyIndiaPvt.Ltd,2009.
3. David A. Bell, "Electronic Instrumentation & Measurements", Oxford University Press PHI 2nd Edition, 2006, ISBN81-203-2360-2.
4. A. D. Helfrick and W.D. Cooper, "Modern Electronic Instrumentation and Measuring Techniques", Pearson, 1st Edition, 2015, ISBN:9789332556065.

Web links and Video Lectures:

1. https://www.classcentral.com/course/swayam-electrical-measurement-and-electronic-instruments-14032
2. https://www.udemy.com/course/electronic-measurements-and-instrumentation/
3. https://nptel.ac.in/courses/108/105/108105153/
4. https://www.classcentral.com/course/powerelectronics-716

B. E. (EC / TC)
ChoiceBasedCreditSystem(CBCS)andOutcomeBasedEducation(OBE) SEMESTER – III

ELECTRONIC DEVICES AND INSTRUMENTATION LABORATORY

Laboratory Code	**18ECL37**	CIE Marks	40
Number of Lecture Hours/Week	02 Hr Tutorial (Instructions) + 02 Hours Laboratory	SEE Marks	60
RBT Level	L1, L2, L3	Exam Hours	03

CREDITS – 02

Course Learning Objectives: This laboratory course enables students to

- Understand the circuit schematic and itsworking.
- Study the characteristics of different electronicdevices.
- Designandtestsimpleelectroniccircuitsasperthespecificationsusingdiscreteelectroniccomponents.
- Familiarize with EDA software which can be used for electronic circuitsimulation.

Laboratory Experiments

PART A : Experiments using Discrete components

1. Conductexperimenttotestdiodeclipping(single/doubleended)andclampingcircuits(positive/negative).
2. HalfwaverectifierandFullwaverectifierwithandwithoutfilterandmeasuretheripplefactor.
3. CharacteristicsofZenerdiodeanddesignaSimpleZenervoltageregulatordeterminelineandloadregulation.
4. Characteristics of LDR and Photo diode and turn on an LED usingLDR
5. Static characteristics ofSCR.
6. SCR Controlled HWR and FWR using RC triggeringcircuit
7. Conductanexperimenttomeasuretemperatureintermsofcurrent/voltageusingatemperaturesensorbridge.
8. Measurement of Resistance using Wheatstone and Kelvin'sbridge.

PART-B : Simulation using EDA software
(EDWinXP, PSpice, MultiSim, Proteus, Circuit Lab or any equivalent tool)

1. InputandOutputcharacteristicsofBJTCommonemitterconfigurationandevaluationofparameters.
2. Transfer and drain characteristics of a JFET andMOSFET.
3. UJT triggering circuit for Controlled Full waveRectifier.
4. Design and simulation of Regulated powersupply.

Course Outcomes: On the completion of this laboratory course, the students will be able to:

- Design and test rectifiers, clipping circuits, clamping circuits and voltage regulators.
- Compute the parameters from the characteristics of power diodes and rectifier circuits using power diodes.
- Analyse the characteristics ofphotodiode,LDR and Temperature sensors.
- Analyse the bridge circuits.
- Analyse characteristics and implement circuits using transistors like BJT,MOSFET,UJT and Regulated power supply through simulation software .

Conduct of Practical Examination:

- All laboratory experiments are to be considered forpracticalexamination.
- Forexaminationonequestionfrom**PART-A**andonequestionfrom**PART-Bor**onlyonequestionfrom **PART-A** experiments based on the complexity, to be set.
- Students are allowed to pick one experiment from thelot.
- Strictlyfollowtheinstructionsasprintedonthecoverpageofanswerscriptforbreakupofmarks.
- ChangeofexperimentisallowedonlyonceandMarksallottedtotheprocedureparttobemadezero.

1. DavidABell,"FundamentalsofElectronicDevicesandCircuitsLabManual,5thEdition,2009,Oxford UniversityPress.
2. MuhammedHRashid,"IntroductiontoPSpiceusingOrCADforcircuitsandelectronics",3rdEdition,Prentice Hall,2003.

B. E. (EC / TC)
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
SEMESTER – III

DIGITAL SYSTEM DESIGN LABORATORY

Laboratory Code	**18ECL38**	**IA Marks**	**40**
Number ofLecture Hours/Week	**02Hr Tutorial (Instructions) + 02 Hours Laboratory**	**Exam Mark**	**60**
		Exam Hour	**03**

CREDITS – 02

Course objectives: This laboratory course enables students to get practical experience in design, realization and verificationof

- Demorgan'sTheorem,SOP,POSforms
- Full/ParallelAdders,SubtractorsandMagnitudeComparator
- Multiplexer usinglogicgates
- Demultiplexers andDecoders
- Flip-Flops, Shift registers andCounters.

NOTE: 1. Use discrete components to test and verify the logic gates. The IC numbers given are suggestive; any equivalent ICs can beused. 2. For experiment No. 11 and 12 any open source or licensed simulation tool may beused.	**Revised Bloom's Taxonomy (RBT) Level**
Laboratory Experiments:	
1. Verify (i) Demorgan'sTheoremfor2variables. (ii) Thesum-ofproductandproduct-of-sumexpressionsusing universalgates.	**L1, L2, L3**
2. Design andimplement (i) Half Adder & Full Adder using i) basic gates. ii) NANDgates (ii) Half subtractor& Full subtractor using i) basic gates ii) NANDgates	**L3, L4**
3.Designandimplement (i) 4-bitParallelAdder/SubtractorusingIC7483. (ii) BCD to Excess-3 code conversion andvice-versa.	**L3, L4**
4. Design and Implementationof (i) 1-bitComparator (ii) 5-bit Magnitude Comparator using IC7485.	**L3, L4**
5. Realize (i) Adder &Subtactors using IC74153. (ii) 4-variable function usingIC74151(8:1MUX).	**L2, L3, L4**
6. Realize (i) Adder &Subtractors using IC74139. (ii) Binary to Gray code conversion & vice-versa (74139)	**L2, L3, L4**
7. Realize the following flip-flops using NANDGates. Master-Slave JK, D & T Flip-Flop.	**L2, L3**
8. Realize the following shift registersusingIC7474/7495 (i) SISO (ii) SIPO (iii)) PISO(iv))PIPO (v) Ring (vi) Johnsoncounter	**L2, L3**

9. Realize(i)DesignMod–NSynchronousUpCounter&DownCounter using 7476 JK Flip-flop (ii) Mod-N Counter using IC7490 /7476 (iii) Synchronous counter usingIC74192	**L2, L3**
10. Design Pseudo Random Sequence generator using7495.	**L2, L3**
11. Design Serial Adder with Accumulator and Simulate using Simulationtool.	**L2, L3, L4**
12. Design Binary Multiplier and Simulate using Simulationtool.	**L2, L3, L4**

Course Outcomes: On the completion of this laboratory course, the students will be able to:

- Identify the truth table of various expressions and combinational circuits using logic gates.
- Design and test various combinational circuits such as adders, subtractors, comparators, multiplexers.
- Develop Boolean expressions using decoders.
- Construct flips-flops, counters and shift registers
- Simulate Serial Binary Adder and Binary Multiplier

Conduct of Practical Examination:

- All laboratory experiments are to be included for practicalexamination.
- Students are allowed to pick one experiment from thelot.
- Strictly follow the instructions as printed on the cover page of answer script for breakup ofmarks.
- Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be madezero.

B. E. (Common to all Programmes) Choice Based Credit System (CBCS) and Outcome Based Education (OBE) SEMESTER –II / III / IV			
Aadalitha Kannada			
Course Code	**18KAK28/39/49**	CIE Marks	100
Teaching Hours/Week (L:T:P)	(0:2:0)		
Credits	01		

ಆಡಳಿತ ಕನ್ನಡ ಕಲಿಕೆಯ ಉದ್ದೇಶಗಳು:

- ಪದವಿ ವಿದ್ಯಾರ್ಥಿಗಳಾಗಿರುವುದರಿಂದ ಆಡಳಿತ ಕನ್ನಡದ ಪರಿಚಯ ಮಾಡಿಕೊಂಡಂತಾಗುವುದು.
- ವಿದ್ಯಾರ್ಥಿಗಳಲ್ಲಿ ಕನ್ನಡ ಭಾಷೆಯ ವ್ಯಾಕರಣದ ಬಗ್ಗೆ ಅರಿವು ಮೂಡಿಸುವುದು.
- ಕನ್ನಡ ಭಾಷಾ ರಚನೆಯಲ್ಲಿನ ನಿಯಮಗಳನ್ನು ಪರಿಚಯಿಸುವುದು.
- ಕನ್ನಡ ಭಾಷಾ ಬಳಕೆಯಲ್ಲಿ ಕಂಡುಬರುವ ದೋಷಗಳು ಹಾಗೂ ಅವುಗಳ ನಿವಾರಣೆ. ಮತ್ತು ರೇಖಾ ಚಿತ್ರಗಳನ್ನು ಪರಿಚಯಿಸುವುದು.
- ಸಾಮಾನ್ಯ ಅರ್ಜಿಗಳು, ಸರ್ಕಾರಿ ಮತ್ತು ಅರೆ ಸರ್ಕಾರಿ ಪತ್ರವ್ಯವಹಾರದ ಬಗ್ಗೆ ಅರಿವು ಮೂಡಿಸುವುದು.
- ಭಾಷಾಂತರ ಮತ್ತು ಪ್ರಬಂಧ ರಚನೆ ಬಗ್ಗೆ ಅರಿವು ಮೂಡಿಸುವುದು.
- ಕನ್ನಡ ಭಾಷಾಧ್ಯಾಯ ಮತ್ತು ಸಾಮಾನ್ಯ ಕನ್ನಡ ಹಾಗೂ ಆಡಳಿತ ಕನ್ನಡದ ಪರಸ್ಪರ ಪರಿಚಯ ಮಾಡಿಕೊಂಡಂತಾಗುವುದು.

ಪರಿವಿಡಿ (ಪಠ್ಯಪುಸ್ತಕದಲ್ಲಿರುವ ವಿಷಯಗಳ ಪಟ್ಟಿ)

ಅಧ್ಯಾಯ – 1 ಕನ್ನಡಭಾಷೆ – ಸಂಕ್ಷಿಪ್ತ ಪರಿಚಯ.
ಅಧ್ಯಾಯ – 2 ಭಾಷಾ ಪ್ರಯೋಗದಲ್ಲಾಗುವ ದೋಷಪರಿಹಾರಗಳು ಮತ್ತು ಅವುಗಳ ನಿವಾರಣೆ.
ಅಧ್ಯಾಯ – 3 ರೇಖಾ ಚಿತ್ರಗಳು ಮತ್ತು ಅವುಗಳ ಉಪಯೋಗ.
ಅಧ್ಯಾಯ – 4 ಪತ್ರ ವ್ಯವಹಾರ.
ಅಧ್ಯಾಯ – 5 ಅರ್ಜಿಗಳು.
ಅಧ್ಯಾಯ – 6 ಸರ್ಕಾರದ ಆದೇಶ ಪತ್ರಗಳು.
ಅಧ್ಯಾಯ – 7 ಸಂಕ್ಷಿಪ್ತ ಪ್ರಬಂಧ ರಚನೆ (ಪ್ರಿನ್ಸಿಸ್ ರೈಟಿಂಗ್), ಪ್ರಬಂಧ ಮತ್ತು ಭಾಷಾಂತರ.
ಅಧ್ಯಾಯ – 8 ಕನ್ನಡ ಕಛೇರಿಗಳು.
ಅಧ್ಯಾಯ – 9 ಕಂಪ್ಯೂಟರ್ ಹಾಗೂ ಮಾಹಿತಿ ತಂತ್ರಜ್ಞಾನ.
ಅಧ್ಯಾಯ – 10 ಪರಿಭಾಷಿಕ ಆಡಳಿತ ಕನ್ನಡ ಪದಗಳು ಮತ್ತು ಇಂಗ್ಲೀಷ್/ ಕಂಪ್ಯೂಟರ್ ಪರಿಭಾಷಿಕ ಪದಗಳು.

ಆಡಳಿತ ಕನ್ನಡ ಕಲಿಕೆಯ ಫಲಿತಾಂಶಗಳು:

- ಆಡಳಿತ ಭಾಷೆ ಕನ್ನಡದ ಪರಿಚಯವಾಗುತ್ತದೆ.
- ವಿದ್ಯಾರ್ಥಿಗಳಲ್ಲಿ ಕನ್ನಡ ಭಾಷೆಯ ವ್ಯಾಕರಣದ ಬಗ್ಗೆ ಅರಿವು ಮೂಡುತ್ತದೆ.
- ಕನ್ನಡ ಭಾಷಾ ರಚನೆಯಲ್ಲಿನ ನಿಯಮಗಳು ಮತ್ತು ರೇಖಾ ಚಿತ್ರಗಳು ಪರಿಚಯಿಸಲ್ಪಡುತ್ತದೆ.
- ಸಾಮಾನ್ಯ ಅರ್ಜಿಗಳು, ಸರ್ಕಾರಿ ಮತ್ತು ಅರೆ ಸರ್ಕಾರಿ ಪತ್ರವ್ಯವಹಾರದ ಬಗ್ಗೆ ಅರಿವು ಮೂಡುತ್ತದೆ.
- ಭಾಷಾಂತರ ಮತ್ತು ಪ್ರಬಂಧ ರಚನೆ ಬಗ್ಗೆ ಅರಿವು ಮೂಡುತ್ತದೆ.
- ಕನ್ನಡ ಭಾಷಾಧ್ಯಾಯ ಮತ್ತು ಸಾಮಾನ್ಯ ಕನ್ನಡ ಹಾಗೂ ಆಡಳಿತ ಕನ್ನಡದ ಪರಸ್ಪರ ಪರಿಚಯಿಸಲ್ಪಡುತ್ತದೆ.

ಪರೀಕ್ಷೆಯ ವಿಧಾನ : ವಿದ್ಯಾರ್ಥಿ ಆಂತರಿಕ ಮೌಲ್ಯಮಾಪನ – ಅರ್ಹತಾ (ಅಂತಿಮವಾಗಿ ಪರಿಗಣಿಸಲಾಗುವುದಿಲ್ಲ ಇದನ್ನು ಗಮನಿಸಿಕೊಳ್ಳಿರಿ):
ಪದವಿ ಮಟ್ಟದಲ್ಲಿನ ಆಂತರಿಕ ಪರೀಕ್ಷೆಯನ್ನು 100 ಅಂಕಗಳಿಗೆ ವಿಶ್ವವಿದ್ಯಾಲಯದ ನಿಯಮಗಳು ಮತ್ತು ನಿರ್ದೇಶನದಂತೆ ನಡೆಸಲ್ಪಡುವುದು.

ಪಠ್ಯಪುಸ್ತಕ : ಆಡಳಿತ ಕನ್ನಡ ಪಠ್ಯ ಪುಸ್ತಕ (ಮುದ್ರಿಸಲಾಗಿರುವ ಸಂಪೂರ್ಣ ಮಾಹಿತಿ ಇರಬೇಕಾದುದು)
ಸಂಪಾದಕರು
ಡಾ. ಎಚ್. ತಿಪ್ಪೇಸ್ವಾಮಿ
ಪ್ರೊ. ವಿ. ಕೇಶವಮೂರ್ತಿ
ಪ್ರಕಾಶಕರು : ಪ್ರಸಾಂಗ, ವಿಶ್ವವಿದ್ಯಾಲಯ ಜಾಕ್ಷಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ, ಬೆಳಗಾವಿ.

B. E. (Common to all Programmes)
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
SEMESTER –II & III/IV

Vyavaharika Kannada

Course Code	**18KVK28/39/49**	CIE Marks	100
Teaching Hours/Week (L:T:P)	(0:2:0)		
Credits	01		

Course Learning Objectives:

The course will enable the students to understand Kannada and communicate in Kannada language.

Table of Contents:

Chapter - 1: Vyavaharika kannada – Parichaya (Introduction to Vyavaharika Kannada).
Chapter - 2: Kannada Aksharamale haagu uchcharane (Kannada Alpabets and Pronunciation).
Chapter - 3: Sambhashanegaagi Kannada Padagalu (Kannada Vocabulary for Communication).
Chapter - 4: Kannada Grammar in Conversations (Sambhashaneyalli Kannada Vyakarana).
Chapter - 5: Activities in Kannada.

Course Outcomes:

At the end of the course, the student will be able to understand Kannada and communicate in Kannada language.

ಪರೀಕ್ಷೆಯ ವಿಧಾನ : ನಿರಂತರ ಆಂತರಿಕ ಮೌಲ್ಯಮಾಪನ – ಅಬಇ **(ಅಟಿಣಟಿಟಿಣಾ ಪಟಿಣಡಿಟಿಬಟಿ ಇಟಿಟಿಣಟಿಣಟಿ):**

ಕಾಲೇಜು ಮಟ್ಟದಲ್ಲಿಯೆ ಆಂತರಿಕ ಪರೀಕ್ಷೆಯನ್ನು 100 ಅಂಕಗಳಿಗೆ ವಿಶ್ವವಿದ್ಯಾಲಯದ ನಿಯಮಗಳು ಮತ್ತು ನಿರ್ದೇಶನದಂತೆ ನಡೆಸತಕ್ಕದ್ದು.

ಪಿಷಾಛಷಿ (ಪಠ್ಯಪುಸ್ತಕ): ವ್ಯಾವಹಾರಿಕ ಕನ್ನಡ ಪಠ್ಯ ಪುಸ್ತಕ (ಗಿಥಿಚಿಟಿಟಿಚಿಟಿಡಿಟಿಣಚಿ ಏಚಿಟಿಟಿಚಿಜಚಿ ಪಿಷಣ ಚಿಣಟಿ)

ಸಂಪಾದಕರು

ಡಾ. ಎಲ್. ತಿಮ್ಮೇಶ
ಪ್ರೊ. ವಿ. ಕೇಶವಮೂರ್ತಿ
ಪ್ರಕಟಣೆ : ಪ್ರಸಾರಾಂಗ, ವಿಶ್ವೇಶ್ವರಯ್ಯ ತಾಂತ್ರಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ, ಬೆಳಗಾವಿ.

B. E. Common to all Programmes
ChoiceBasedCreditSystem(CBCS)andOutcomeBasedEducation(OBE) SEMESTER - III

CONSTITUTION OF INDIA, PROFESSIONAL ETHICS AND CYBER LAW (CPC)

Course Code	**18CPC39/49**	CIE Marks	40
Teaching Hours/Week (L:T:P)	(1:0:0)	SEE Marks	60
Credits	01	Exam Hours	02

Course Learning Objectives: To

- know the fundamental political codes, structure, procedures, powers, and duties of Indian governmentinstitutions,fundamentalrights,directiveprinciples,andthedutiesofcitizens
- Understand engineering ethics and their responsibilities; identify their individual roles and ethical responsibilities towards society.
- Know about the cybercrimes and cyber laws for cyber safetymeasures.

Module-1

Introduction to Indian Constitution:
TheNecessityoftheConstitution,TheSocietiesbeforeandaftertheConstitutionadoption.Introductiontothe Indian constitution, The Making of the Constitution, The Role of the Constituent Assembly - Preamble and SalientfeaturesoftheConstitutionofIndia.FundamentalRightsanditsRestrictionandlimitationsindifferent Complex Situations. Directive Principles of State Policy (DPSP) and its present relevance inour society with examples. Fundamental Duties and its Scope and significance in Nation building.

Module-2

Union Executive and State Executive:
Parliamentary System, Federal System, Centre-State Relations. Union Executive – President, Prime Minister, Union Cabinet, Parliament - LS and RS, Parliamentary Committees, Important Parliamentary Terminologies. SupremeCourtofIndia,JudicialReviewsandJudicialActivism.StateExecutives–Governor,ChiefMinister, State Cabinet, State Legislature, High Court and Subordinate Courts, Special Provisions(Articles 370.371,371J) for some States.

Module-3

Elections, Amendments and Emergency Provisions:
Elections, Electoral Process, and Election Commission of India, Election Laws. Amendments - Methods in Constitutional Amendments (How and Why) and Important Constitutional Amendments. Amendments – 7,9,10,12,42,44, 61, 73,74, ,75, 86, and 91,94,95,100,101,118 and some important Case Studies. Emergency Provisions, types of Emergencies and itsconsequences.

Constitutional special provisions:
Special Provisions for SC and ST, OBC, Women, Children and Backward Classes.

Module-4

Professional / Engineering Ethics:
Scope & Aims of Engineering & Professional Ethics - Business Ethics, Corporate Ethics, Personal Ethics. Engineering and Professionalism, Positive and Negative Faces of Engineering Ethics, Code of Ethics as defined in the website of Institution of Engineers (India): Profession, Professionalism, and Professional Responsibility. Clash of Ethics, Conflicts of Interest. Responsibilities in Engineering Responsibilities in Engineering and Engineering Standards, the impediments to Responsibility. Trust and Reliability in Engineering, IPRs (Intellectual Property Rights), Risks, Safety and liability in Engineering

Module-5

Internet Laws, Cyber Crimes and Cyber Laws:
Internet and Need for Cyber Laws, Modes of Regulation of Internet, Types of cyber terror capability, Net neutrality, Types of Cyber Crimes, India and cyber law, Cyber Crimes and the information Technology Act 2000, Internet Censorship. Cybercrimes and enforcement agencies.

Course Outcomes: On completion of this course, students will be able to,

CO 1: Have constitutional knowledge and legal literacy.

CO 2: Understand Engineering and Professional ethics and responsibilities of Engineers.

CO 3: Understand the the cybercrimes and cyber laws for cyber safety measures.

Question paper pattern for SEE and CIE:

- The SEE question paper will be set for 100 marks and the marks scored by the students will proportionately be reduced to 60. The pattern of the question paper will be objective type (MCQ).
- For the award of 40 CIE marks, refer the University regulations2018.

Sl. No.	Title of the Book	Name of the Author/s	Name of the Publisher	Edition and Year
Textbook/s				
1	Constitution of India, Professional Ethics and Human Rights	Shubham Singles, Charles E. Haries, and et al	Cengage Learning India	2018
2	Cyber Security and Cyber Laws	Alfred Basta and et al	Cengage Learning India	2018
Reference Books				
3	Introduction to the Constitution of India	Durga Das Basu	Prentice –Hall,	2008.
4	Engineering Ethics	M. Govindarajan, S. Natarajan, V. S. Senthilkumar	Prentice –Hall,	2004

B. E. Common to all Programmes
ChoiceBasedCreditSystem(CBCS)andOutcomeBasedEducation(OBE) SEMESTER - III

ADDITIONAL MATHEMATICS – I

(Mandatory Learning Course: Common to All Programmes)
(A Bridge course for Lateral Entry students under Diploma quota to BE/B.Tech. programmes)

Course Code	**18MATDIP31**	CIE Marks	40
Teaching Hours/Week (L:T:P)	(2:1:0)	SEE Marks	60
Credits	0	Exam Hours	03

Course Learning Objectives:

- To provide basic concepts of complex trigonometry, vector algebra, differential and integral calculus.
- To provide an insight into vector differentiation and first orderODE's.

Module-1

Complex Trigonometry: Complex Numbers: Definitions and properties. Modulus and amplitude of a complex number, Argand's diagram, De-Moivre's theorem (without proof).
Vector Algebra: Scalar and vectors. Addition and subtraction and multiplication of vectors- Dot and Cross products, problems.

Module-2

Differential Calculus: Review of elementary differential calculus. Polar curves –angle between the radius vector and the tangent pedal equation- Problems. Maclaurin's series expansions, problems.
Partial Differentiation: Euler's theorem for homogeneous functions of two variables. Total derivatives - differentiation of composite function. Application to Jacobians of order two.

Module-3

VectorDifferentiation: Differentiationofvectorfunctions.Velocityandaccelerationofaparticlemovingon aspacecurve.Scalarandvectorpointfunctions.Gradient,Divergence,CurlandLaplacian(Definitionsonly). Solenoidal and irrotational vectorfields-Problems.

Module-4

IntegralCalculus: Reviewofelementaryintegralcalculus.Statementofreductionformulaefor $\sin^n x, \cos^n x,$ and $\sin^N x \times \cos^n x$ andevaluationofthesewithstandardlimits-Examples.Doubleandtripleintegrals,problems.

Module-5

Ordinary differential equations (ODE's): Introduction-solutions of first order and first degree differential equations: Variable Separable methods, exact and linear differential equations of order one. Application to Newton's law of cooling.

Course Outcomes: At the end of the course the student will be able to:

- CO1: Apply concepts of complex numbers and vector algebra to analyze the problems arising in relatedarea.
- CO2: Use derivatives and partial derivatives to calculate rate of change of multivariate functions.
- CO3: Analyze position, velocity and acceleration in two and three dimensions of vector valued functions. CO4: Learn techniques of integration including the evaluation of double and tripleintegrals.
- CO5: Identify and solve first order ordinary differentialequations.

Question paper pattern:

3. The question paper will have ten full questions carrying equalmarks.
4. Each full question will be for 20marks.

- Therewillbetwofullquestions(withamaximumoffoursub-questions)fromeachmodule.

Sl. No.	Title of the Book	Name of the Author/s	Name of the Publisher	Edition and Year
Textbook				
1	Higher Engineering Mathematics	B.S. Grewal	Khanna Publishers	43rd Edition, 2015
Reference Books				
1	Advanced Engineering Mathematics	E. Kreyszig	John Wiley & Sons	10th Edition, 2015
2	Engineering Mathematics Vol.I	RohitKhurana	Cengage Learinng	2015

K.S.INSTITUTE OF TECHNOLOGY, BANGALORE

(AFFLIATED TO VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELGAUM)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGG.

TECHNOLOGICAL INNOVATION MANAGEMENT AND ENTREPRENEURSHIPV

Course Title: M&E **Course Code :**
18ES51Credits:03 **L-T-P :4-0-0**
Contact Hours/Week: 03 **Total Hours:50**
Exam. Marks:100 **IA Marks :30**
Exam. Hours : 03

Course Learning Objectives: This course will enable students to:

- Understand basic skills ofManagement
- Understand the need for Entrepreneurs and theirskills
- Identify the Management functions and Socialresponsibilities
- UnderstandtheIdeationProcess,creationofBusinessModel,FeasibilityStudyandsourcesoffunding

Module-1	RBT Level
Management: Nature and Functions of Management – Importance, Definition, Management Functions, Levels of Management, Roles of Manager, Managerial Skills, Management & Administration, Management as a Science, Art &**Profession (Selected topics of Chapter 1, Text 1).** **Planning:** Planning-Nature, Importance, Types, Steps and Limitations of Planning; Decision Making – Meaning, Types and Steps in Decision Making(**Selected topics from Chapters 4 & 5, Text 1).**	**L1,L2**
Module-2	
Organizing and Staffing: Organization-Meaning, Characteristics, Process of Organizing, Principles of Organizing, Span of Management (meaning and importance only), Departmentalisation, Committees–Meaning, Types of Committees; Centralization Vs DecentralizationofAuthorityandResponsibility;**Staffing**-NeedandImportance**,**Recruitmentand Selection Process **(Selected topics from Chapters 7, 8 & 11,Text1).** **Directing and Controlling:** Meaning and Requirements of Effective Direction, Giving Orders; Motivation-Nature of Motivation, Motivation Theories (Maslow's Need-Hierarchy Theory and Herzberg's Two Factor Theory); Communication – Meaning, Importance and Purposes of Communication; Leadership-Meaning, Characteristics, Behavioural Approach of Leadership; Coordination-Meaning, Types, Techniques of Coordination; Controlling – Meaning, Need for Control System, Benefits of Control, Essentials of Effective Control System, Steps in Control Process (**Selected topics from Chapters 15 to 18 and 9, Text 1).**	**L1,L2**
Module-3	
Social Responsibilities of Business: Meaning of Social Responsibility, Social Responsibilities of Business towards Different Groups, Social Audit, Business Ethics and Corporate Governance **(Selected topics from Chapter 3, Text 1).** **Entrepreneurship**: Definition of Entrepreneur, Importance of Entrepreneurship, concepts of Entrepreneurship, Characteristics of successful Entrepreneur, Classification of Entrepreneurs, Myths of Entrepreneurship, Entrepreneurial Development models, Entrepreneurial development cycle, Problems faced by Entrepreneurs and capacity building for Entrepreneurship **(Selected topics from Chapter 2, Text 2).**	**L1,L2**
Module-4	
Family Business: Role and Importance of Family Business, Contributions of Family Business in India, Stages of Development of a Family Business, Characteristics of a Family-owned Business in India, Various types of family businesses **(Selected topics from Chapter 4,(Page 71-75) Text 2).** **Idea Generation and Feasibility Analysis-** Idea Generation; Creativity and Innovation; Identification of Business Opportunities; Market Entry Strategies; Marketing Feasibility; Financial Feasibilities; Political Feasibilities; Economic Feasibility; Social and Legal Feasibilities; Technical Feasibilities; Managerial Feasibility, Location and Other Utilities Feasibilities.**(Selected topics from Chapter 6(Page No. 111-117) & Chapter 7(Page No. 140-142), Text 2)**	**L1,L2**

Module-5	
Business model – Meaning, designing, analyzing and improvising; Business Plan – Meaning, Scope and Need; Financial, Marketing, Human Resource and Production/Service Plan; Business plan Formats; Project report preparation and presentation; Why some Business Plan fails? **(Selected topics from Chapter 8 (Page No 159-164, Text 2)** **Financing and How to start a Business?** Financial opportunity identification; Banking sources; Nonbanking Institutions and Agencies; Venture Capital – Meaning and Role in Entrepreneurship; Government Schemes for funding business; Pre launch, Launch and Post launch requirements; Procedure for getting License and Registration; Challenges and Difficulties in Starting an Enterprise**(Selected topics from Chapter 7(Page No 147-149), Chapter 5(Page No 93-99) & Chapter 8(Page No. 166-172) Text 2)** **Project Design and Network Analysis:** Introduction, Importance of Network Analysis, Origin of PERT and CPM, Network, Network Techniques, Need for Network Techniques, Steps in PERT, CPM, Advantages, Limitations and Differences**. (Selected topics from Chapters 20, Text 3).**	**L1,L2,L 3**

Course Outcomes: After studying this course, students will be able to:

- Identify the different fundamental concepts of Management and Entrepreneurship.
- Select the best Entrepreneurship model for the required domain of establishment.
- Explain the functions of Managers, Entrepreneurs and their social responsibilities.
- Survey the Institutional support by various state and central government agencies.
- Apply the knowledge of Project Formulation and Evaluation Techniques

Text Books:

1. Principles of Management – P.C Tripathi, P.N Reddy, McGraw Hill Education, 6th Edition, 2017. ISBN-13:978-93-5260-535-4.
2. Entrepreneurship Development Small Business Enterprises- Poornima M Charantimath, Pearson Education 2008, ISBN978-81-7758-260-4.
3. DynamicsofEntrepreneurialDevelopmentandManagementbyVasantDesai.HPH2007,ISBN:978- 81-8488-801-2.
4. RobertD.Hisrich,MathewJ.Manimala,MichaelPPetersandDeanA.Shepherd,"Entrepreneurship", 8th Edition, Tata Mc-graw Hill Publishing Co.ltd.-new Delhi, 2012

Reference Book:

1. Essentials of Management: An International, Innovation and Leadership perspective by Harold Koontz, Heinz Weihrich McGraw Hill Education, 10th Edition 2016. ISBN- 978-93-392-2286-4.

B. E. (EC / TC)
ChoiceBasedCreditSystem(CBCS)andOutcomeBasedEducation(OBE) SEMESTER – V

DIGITAL SIGNAL PROCESSING

Course Code	**18EC52**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**3+2(Tutorial)**	**SEE Marks**	**60**
		Exam Hours	**03**

CREDITS – 04

Course Learning Objectives: This course will enable students to

- Understandthefrequencydomainsamplingandreconstructionofdiscretetimesignals.
- Studythepropertiesandthedevelopmentofefficientalgorithmsforthecomputationof DFT.
- Realization of FIR and IIR filters in different structuralforms.
- Learn the procedures to design of IIR filters from the analog filters using impulse invariance and bilinear transformation.
- Study the different windows used in the design of FIR filters and design appropriate filters based on the specifications.
- Understand the architecture and working of DSPprocessor

Module-1	**RBT Level**
Discrete Fourier Transforms (DFT): Frequency domain sampling and Reconstruction of Discrete Time Signals, The Discrete Fourier Transform, DFT as a linear transformation, Properties of the DFT: Periodicity, Linearity and Symmetry properties, Multiplication of two DFTs and Circular Convolution, Additional DFT properties. **[Text 1]**	**L1,L2, L3**
Module-2	
Linear filtering methods based on the DFT: Use of DFT in Linear Filtering, Filtering of Long data Sequences. **Fast-Fourier-Transform (FFT) algorithms:** Efficient Computation of the DFT: Radix-2 FFT algorithms for the computation of DFT and IDFT–decimation-in-time and decimation-in-frequency algorithms. **[Text 1]**	**L1,L2, L3**
Module-3	
Design of FIR Filters: Characteristics of practical frequency –selective filters, Symmetric and Antisymmetric FIR filters, Design of Linear-phase FIR filters using windows - Rectangular, Hamming, Hanning, Bartlett windows. Design of FIR filters using frequency sampling method. Structure for FIR Systems: Direct form, Cascade form and Lattice structures**.[Text1]**	**L1,2,L3**
Module-4	
IIR Filter Design: Infinite Impulse response Filter Format, Bilinear Transformation Design Method, Analog Filters using Lowpass prototype transformation, Normalized Butterworth Functions, Bilinear Transformation and Frequency Warping, Bilinear Transformation Design Procedure, Digital Butterworth Filter Design using BLT. Realization of IIR Filters in Direct form I and II. **[Text 2]**	**L1,L2,L3**
Module-5	
Digital Signal Processors: DSP Architecture, DSP Hardware Units, Fixed point format, Floating point Format, IEEE Floating point formats, Fixed point digital signal processors, Floating point processors, FIR and IIR filter implementations in Fixed point systems**. [Text 2]**	**L1,L2, L3**

Course Outcomes: After studying this course, students will be able to:

- Construct the frequency domain sampling and reconstruction of discrete time signals.
- Make use of the properties and develop efficient algorithms for the computation of DFT.
- Construct FIR and IIR filters in different structural forms.
- Utilize the procedures to design IIR filters from the analog filters using impulse invariance and bilinear transformation.
- Identify the different windows used in the design of FIR filters and design appropriate filters based on the specifications.

Question paperpattern:

- Examinationwillbeconductedfor100markswithquestionpapercontaining10fullquestions,eachof20 marks.
- Each full question can have a maximum of 4 subquestions.
- Therewillbe2fullquestionsfromeachmodulecoveringallthetopicsofthemodule.
- Studentswillhavetoanswer5fullquestions,selectingonefullquestionfromeachmodule.
- Thetotalmarkswillbeproportionallyreduced to60marksasSEEmarksis60

Text Book:

1. Proakis&Monalakis, "Digital signal processing – Principles Algorithms & Applications", 4th Edition, Pearson education, New Delhi, 2007. ISBN:81-317-1000-9.
2. LiTan,JeanJiang,"DigitalSignalprocessing–FundamentalsandApplications",AcademicPress,2013, ISBN:978-0-12-415893.

Reference Books:

1. Sanjit K Mitra, "Digital Signal Processing, A Computer Based Approach", 4th Edition, McGraw Hill Education,2013,
2. Oppenheim & Schaffer, "Discrete Time Signal Processing" , PHI,2003.
3. D.GaneshRao and Vineeth P Gejji, "Digital Signal Processing" Cengage India Private Limited, 2017, ISBN:9386858231

B. E. (EC / TC)
ChoiceBasedCreditSystem(CBCS)andOutcomeBasedEducation(OBE) SEMESTER – V

PRINCIPLES OF COMMUNICATION SYSTEMS

Subject Code	**18EC53**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**3+2 (Tutorial)**	**SEE Marks**	**60**
		Exam Hours	**03**

CREDITS – 04

Course Learning Objectives: This course will enable students to

- Understand and analyse concepts of Analog Modulation schemes viz; AM, FM., Low pass sampling and Quantization as a randomprocess.
- Understandandanalyseconceptsdigitizationofsignalsviz;sampling,quantizingandencoding.
- Evolve the concept of SNR in the presence of channel induced noise and study Demodulation of analog modulatedsignals.
- Evolve the concept of quantization noise for sampled and encoded signals and study the concepts of reconstruction from these samples at areceiver.

Module-1	**RBT Level**
AMPLITUDEMODULATION: Introduction,AmplitudeModulation:Time&FrequencyDomain description, Switching modulator, Envelop detector. **(3.1 – 3.2 inText)** **DOUBLE SIDE BAND-SUPPRESSED CARRIER MODULATION:** Time and Frequency Domain description, Ring modulator, Coherent detection, Costas Receiver, Quadrature Carrier Multiplexing. **(3.3 – 3.4 in Text)** **SINGLE SIDE–BAND AND VESTIGIAL SIDEBAND METHODS OF MODULATION:** SSB Modulation, VSB Modulation, Frequency Translation, Frequency- Division Multiplexing,Theme Example: VSB Transmission of Analog and Digital Television. **(3.5 – 3.8 in Text)**	**L1, L2, L3**
Module-2	
ANGLE MODULATION: Basic definitions, Frequency Modulation: Narrow Band FM, Wide BandFM,TransmissionbandwidthofFMSignals,GenerationofFMSignals,DemodulationofFM Signals, FM Stereo Multiplexing, Phase–Locked Loop: Nonlinear model of PLL, Linear model of PLL,NonlinearEffectsinFMSystems.TheSuperheterodyneReceiver**(4.1–4.6ofText)**	**L1, L2,L3**
Module-3	
[Review of Mean, Correlation and Covariance functions of Random Processes. ***(No questions to be set on these topics)]*** **NOISE** - Shot Noise, Thermal noise, White Noise, Noise Equivalent Bandwidth **(5.10 in Text)** **NOISE IN ANALOG MODULATION:** Introduction, Receiver Model, Noise in DSB-SC receivers. Noise in AM receivers, Threshold effect, Noise in FM receivers, Capture effect, FM threshold effect, FM threshold reduction, Pre-emphasis and De-emphasis in FM **(6.1 – 6.6 in Text)**	**L1, L2,L3**
Module-4	
SAMPLING AND QUANTIZATION: Introduction, Why Digitize Analog Sources?, The Low pass Sampling process Pulse Amplitude Modulation. Time Division Multiplexing, Pulse-Position Modulation, Generation of PPM Waves, Detection of PPM Waves.**(7.1 – 7.7 in Text)**	**L1, L2,L3**
Module-5	
SAMPLING AND QUANTIZATION (Contd): The Quantization Random Process, Quantization Noise, Pulse–Code Modulation: Sampling, Quantization, Encoding, Regeneration, Decoding, Filtering, Multiplexing; Delta Modulation **(7.8 – 7.10 in Text)**, Application examples - (a) Video + MPEG **(7.11 in Text)** and (b) Vocoders**(refer Section 6.8 of Reference Book 1)**.	**L1, L2,L3**

Course Outcomes: After studying this course, students will be able to:

- Apply the time and frequency domain knowledge for the generation and demodulation of amplitude modulated signals.
- Identify the performance of different generation and detection methodologies of AM, FM and multiplexing.
- Utilize analog signals in time domain as random processes and identify the types of basic Noise
- Identify the influence of noise in receivers of analog modulated signals
- Compare the characteristics of pulse modulation techniques.

Question paper pattern:

- Examinationwillbeconductedfor100markswithquestionpapercontaining10fullquestions,eachof 20marks.
- Each full question can have a maximum of 4 subquestions.
- Therewillbe2fullquestionsfromeachmodulecoveringallthetopicsofthemodule.
- Studentswillhavetoanswer5fullquestions,selectingonefullquestionfromeachmodule.
- Thetotalmarkswillbeproportionallyreducedto60 marksasSEEmarksis60.

Text Book:

"Communication Systems", Simon Haykins&Moher, 5th Edition, John Willey, India Pvt. Ltd, 2010, ISBN 978 – 81 – 265 – 2151 – 7.

Reference Books:

1. Modern Digital and Analog Communication Systems, B. P. Lathi, Oxford University Press., 4th edition.
2. An Introduction to Analog and Digital Communication, Simon Haykins, John Wiley India Pvt. Ltd., 2008, ISBN978–81–265–3653–5.
3. Principles of Communication Systems, H.Taub&D.L.Schilling,TMH,2011.
4. CommunicationSystems,HaroldP.E,SternSamyandA.Mahmond,PearsonEdition,2004.

B. E. (EC / TC) ChoiceBasedCreditSystem(CBCS)andOutcomeBasedEducation(OBE) SEMESTER – V			
INFORMATION THEORY and CODING			
Course Code	**18EC54**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**3**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (8 Hours / Module)**	**Exam Hours**	**03**
CREDITS – 03			

Course Learning Objectives: This course will enable students to

- Understand the concept of Entropy, Rate of information and order of the source with reference to dependent and independentsource.
- Study various source encodingalgorithms.
- Model discrete & continuous communicationchannels.
- Study various error control codingalgorithms.

Module-1	**RBT Level**
Information Theory: Introduction, Measure of information, Information content of message, Average Information content of symbols in Long Independent sequences, Average Information content of symbols in Long dependent sequences, Markov Statistical Model for Information Sources, Entropy and Information rate of Markoff Sources **(Section 4.1, 4.2 of Text 1)**	**L1, L2,L3**
Module-2	
Source Coding: Encoding of the Source Output, Shannon's Encoding Algorithm**(Sections 4.3, 4.3.1 of Text 1),** Shannon Fano Encoding Algorithm **(Section 2.15 of Reference Book 4)** Source coding theorem, Prefix Codes, Kraft McMillan Inequality property – KMI, Huffman codes **(Section 2.2 of Text 2)**	**L1, L2,L3**
Module-3	
Information Channels: Communication Channels, Discrete Communication channels Channel Matrix, Joint probabilty Matrix, Binary Symmetric Channel, System Entropies. **(Section 4.4, 4.5, 4.51,4.5.2 of Text 1)** Mutual Information, Channel Capacity, Channel Capacity of Binary Symmetric Channel, **(Section 2.5, 2.6 of Text 2)** Binary Erasure Channel, Muroga,s Theorem **(Section 2.27, 2.28 of Reference Book 4)**	**L1, L2, L3**
Module-4	
Error Control Coding: Introduction, Examples of Error control coding, methods of Controlling Errors, Types of Errors, types of Codes, Linear Block Codes: matrix description of Linear Block Codes, Error detection & Correction capabilities of Linear Block Codes, Single error correction Hamming code, Table lookup Decoding using Standard Array. **Binary Cyclic Codes:** Algebraic Structure of Cyclic Codes, Encoding using an (n-k) Bit Shift register, Syndrome Calculation, Error Detection and Correction **(Sections 9.1, 9.2,9.3,9.3.1,9.3.2,9.3.3 of Text 1)**	**L1, L2, L3**
Module-5	
Convolution Codes: Convolution Encoder, Time domain approach, Transform domain approach, Code Tree, Trellis and State Diagram, The Viterbi Algorithm) **(Section 8.5 – Articles 1,2 and 3, 8.6- Article 1 of Text 2)**	**L1, L2, L3**

Course Outcomes: After studying this course, students will be able to:

- Make use of the concepts of dependent & independent source to measure the information, entropy, rate of information and order of a source.
- Construct the information codes using Shannon Encoding, Shannon Fano, Prefix and Huffman Encoding Algorithms.
- Model the continuous and discrete communication channels using input, output and joint probabilities.
- Develop a codeword comprising of the check bits computed using Linear Block codes, cyclic codes & convolution codes
- Examine the encoding and decoding circuits for Linear Block codes, cycliccodes, convolution codes, BCH and Golay codes.

- Design the encoding and decoding circuits for Linear Block codes, cyclic codes, convolutional codes, BCH and Golaycodes.

Question paper pattern:

- Examinationwillbeconductedfor100markswithquestionpapercontaining10fullquestions,eachof 20marks.
- Each full question can have a maximum of 4 subquestions.
- Therewillbe2fullquestionsfromeachmodulecoveringallthetopicsofthemodule.
- Studentswillhavetoanswer5fullquestions,selectingonefullquestionfromeachmodule.
- Thetotalmarkswillbeproportionallyreduced to60 marksasSEEmarksis60.

Text Book:

1. Digitalandanalogcommunicationsystems,K.SamShanmugam,JohnWileyIndiaPvt.Ltd,1996.
2. Digital communication, Simon Haykin, John Wiley India Pvt. Ltd,2008.

Reference Books:

1. ITC and Cryptography, Ranjan Bose, TMH, II edition,2007
2. Principlesofdigitalcommunication,J.Das,S.K.Mullick,P.K.Chatterjee,Wiley,1986-Technology &Engineering
3. Digital Communications – Fundamentals and Applications, Bernard Sklar, Second Edition, Pearson Education, 2016, ISBN:9780134724058.
4. Information Theory and Coding, HariBhat, Ganesh Rao, Cengage,2017.
5. Error Correction Coding by Todd K Moon,Wiley Std. Edition,2006

B. E. (EC / TC)
ChoiceBasedCreditSystem(CBCS)andOutcomeBasedEducation(OBE) SEMESTER – V

ELECTROMAGNETIC WAVES

Course Code	**18EC55**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (8 Hours per Module)**	**Exam Hours**	**03**

CREDITS – 03

Course Learning Objectives: This course will enable students to:

- Studythedifferentcoordinatesystems,PhysicalsignificanceofDivergence,CurlandGradient.
- Understand the applications of Coulomb's law and Gauss law to different charge distributions and the applications of Laplace's and Poisson's Equations to solve real time problems on capacitance of different chargedistributions.
- Understand the physical significance of Biot-Savart's, Amperes's Law and Stokes'theorem for different currentdistributions.
- Infer the effects of magnetic forces, materials andinductance.
- Know the physical interpretation of Maxwell' equations and applications for Plane waves for their behavior in differentmedia.
- Acquire knowledge of Poynting theorem and its application of powerflow.

Module-1	**RBT Level**
Revision of Vector Calculus – **(Text 1: Chapter 1)** **Coulomb's Law, Electric Field Intensity and Flux density**: Experimental law of Coulomb, Electric field intensity, Field due to continuous volume charge distribution, Field of a line charge, FielddduetoSheetofcharge,Electricfluxdensity,NumericalProblems.**(Text:Chapter2.1to2.5, 3.1)**	**L1, L2, L3**
Module -2	
Gauss's law and Divergence: Gauss 'law, Application of Gauss' law to point charge, line charge, Surface charge and volume charge, Point (differential) form of Gauss law, Divergence. Maxwell's First equation (Electrostatics), Vector Operator ▼ and divergence theorem, Numerical Problems (**Text: Chapter 3.2 to 3.7).** **Energy, Potential and Conductors**: Energy expended or work done in moving a point charge in an electric field, The line integral, Definition of potential difference and potential, The potential field of point charge, Potential gradient, Numerical Problems **(Text: Chapter 4.1 to 4.4 and 4.6).**Current and Current density, Continuity of current. **(Text: Chapter 5.1, 5.2)**	**L1, L2, L3**
Module-3	
Poisson'sandLaplace'sEquations:DerivationofPoisson'sandLaplace'sEquations,Uniqueness theorem,ExamplesofthesolutionofLaplace'sequation,NumericalproblemsonLaplaceequation **(Text: Chapter 7.1 to7.3)** **SteadyMagneticField**:Biot-SavartLaw,Ampere'scircuitallaw,Curl,Stokes'theorem,Magnetic flux and magnetic flux density, Basic concepts Scalar and Vector Magnetic Potentials,Numerical problems. (**Text: Chapter 8.1 to 8.6)**	**L1, L2, L3**
Module -4	
Magnetic Forces: Force on a moving charge, differential current elements, Force between differential current elements, Numerical problems **(Text: Chapter 9.1 to 9.3).** **Magnetic Materials**: Magnetization and permeability, Magnetic boundary conditions, The magnetic circuit, Potential energy and forces on magnetic materials, Inductance and mutual reactance, Numerical problems **(Text: Chapter 9.6 to 9.7).** Faraday' law of Electromagnetic Induction –Integral form and Point form, Numerical problems **(Text: Chapter 10.1)**	**L1, L2, L3**
Module -5	
Maxwell's equations Continuity equation, Inconsistency of Ampere's law with continuity equation, displacement current, Conduction current, Derivation of Maxwell's equations in point form, and integral form, Maxwell's equations for different media, Numerical problems **(Text: Chapter 10.2 to 10.4)** **Uniform Plane Wave**: Plane wave, Uniform plane wave, Derivation of plane wave equations from	**L1, L2, L3**

Maxwell's equations, Solution of wave equation for perfect dielectric, Relation between E and H, Wave propagation in free space, Solution of wave equation for sinusoidal excitation, wave propagation in any conducting media (**γ, α, β, η**) and good conductors, Skin effect or Depth of penetration, Poynting's theorem and wave power, Numerical problems. **(Text: Chapter 12.1 to 12.4)**	

Course Outcomes: After studying this course, students will be able to:

- Interpret the problems on electric field due to point, linear, volume charges by applying conventional methods or by Gauss law.
- Analyze potential and energy with respect to point charge and capacitance using Laplace equation.
- Solve for magnetic field, force, and potential energy of magnetic materials.
- Apply Maxwell 's equation for time varying fields, EM waves in free space and conductors.
- Make use of Poynting theorem to find power associated with EM waves.

Question paper pattern:

- Examinationwillbeconductedfor100markswithquestionpapercontaining10fullquestions,eachof 20marks.
- Each full question can have a maximum of 4 subquestions.
- Therewillbe2fullquestionsfromeachmodulecoveringallthetopicsofthe module.
- Studentswillhavetoanswer5fullquestions,selectingonefullquestionfromeachmodule.
- Thetotalmarkswillbeproportionallyreducedto60 marksasSEEmarksis60.

Text Book:

W.H.HaytandJ.A.Buck,—EngineeringElectromagnetics,8thEdition,TataMcGraw- Hill, 2014,ISBN-978-93-392-0327-6.

Reference Books:

1. ElementsofElectromagnetics–MatthewN.O.,Sadiku,Oxforduniversitypress,4th Edn.
2. ElectromagneticWavesandRadiatingsystems–E.C.JordanandK.G.Balman,PHI, 2nd Edn.
3. Electromagnetics- Joseph Edminister, Schaum Outline Series, McGrawHill.
   N.NarayanaRao,—FundamentalsofElectromagneticsforEngineering,Pearson.

B. E. (EC / TC)
ChoiceBasedCreditSystem(CBCS)andOutcomeBasedEducation(OBE) SEMESTER – V

Verilog HDL

Course Code	**18EC56**	**IA Marks**	**40**
Number of Lecture Hours/Week	**03**	**Exam Marks**	**60**
Total Number of Lecture Hours	**40 (08 Hours per Module)**	**Exam Hours**	**03**

CREDITS– 03

Course Learning Objectives:

- Learn different Verilog HDLconstructs.
- Familiarize the different levels of abstraction inVerilog.
- Understand Verilog Tasks, Functions andDirectives.
- Understand timing and delaySimulation.
- Understand the concept of logic synthesis and its impact inverification

Module 1	**RBT Level**
Overview of Digital Design with Verilog HDL: Evolution of CAD, emergence of HDLs, typical HDL-flow, why Verilog HDL?, trends in HDLs. **Hierarchical Modeling Concepts:** Top-down and bottom-up design methodology, differences between modules and module instances, parts of a simulation, design block, stimulus block.	**L1,L2,L3**
Module 2	
Basic Concepts: Lexical conventions, data types, system tasks, compiler directives. **Modules and Ports:** Module definition, port declaration, connecting ports, hierarchical name referencing.	**L1,L2,L3**
Module 3	
Gate-Level Modeling: Modeling using basic Verilog gate primitives, description of and/or and buf/not type gates, rise, fall and turn-off delays, min, max, and typical delays. **Dataflow Modeling:** Continuous assignments, delay specification, expressions, operators, operands, operator types.	**L1,L2,L3**
Module 4	
Behavioral Modeling: Structured procedures, initial and always, blocking and non-blocking statements, delay control, generate statement, event control, conditional statements, Multiway branching, loops, sequential and parallel blocks. **Tasks and Functions:** Differences between tasks and functions, declaration, invocation, automatic tasks and functions.	**L1,L2,L3**
Module 5	
Useful Modeling Techniques: Procedural continuous assignments, overriding parameters, conditional compilation and execution, useful system tasks. **Logic Synthesis with Verilog:** Logic Synthesis, Impact of logic synthesis, Verilog HDL Synthesis, Synthesis design flow, Verification of Gate-Level Netlist**. (Chapter 14 till 14.5 of Text).**	**L1,L2,L3**

Course Outcomes: At the end of this course, students should be able to

- Develop Verilog programs in gate, dataflow (RTL), behavioral and switch modeling levels of Abstraction & simple programs in VHDL in different styles.
- Identify the suitable Abstraction level for a particular digital design. ·
- Develop the programs more effectively using Verilog tasks and directives.
- Develop Verilog code for timing and delay Simulation
- Develop and verify the functionality of digital circuit/system using test benchesusing VHDL and Verilog

Question paper pattern:

- Examinationwillbeconductedfor100markswithquestionpapercontaining10fullquestions,eachof 20marks.
- Each full question can have a maximum of 4 subquestions.
- Therewillbe2fullquestionsfromeachmodulecoveringallthetopicsofthe module.
- Studentswillhavetoanswer5fullquestions,selectingonefullquestionfromeachmodule.

- Thetotalmarkswillbeproportionallyreduced to60 marksasSEEmarksis60.

Text Book:

Samir Palnitkar, "**Verilog HDL: A Guide to Digital Design and Synthesis"**, Pearson Education, Second Edition.

Reference Books:

1. Donald E. Thomas, Philip R. Moorby, "The Verilog Hardware Description Language", Springer Science+Business Media, LLC, Fifthedition.
2. Michael D. Ciletti, "Advanced Digital Design with the Verilog HDL" Pearson (Prentice Hall), Second edition.
3. Padmanabhan,TripuraSundari,"DesignthroughVerilogHDL",Wiley,2016orearlier.

B. E. (EC / TC)
ChoiceBasedCreditSystem(CBCS)andOutcomeBasedEducation(OBE) SEMESTER – V

DIGITAL SIGNAL PROCESSING LABORATORY

Course Code	**18ECL57**	**IA Marks**	**40**
Number of Lecture Hours/Week	**02Hr Tutorial (Instructions) + 02 Hours Laboratory**	**Exam marks**	**60**
RBT Level	**L1, L2, L3**	**Exam Hours**	**03**

CREDITS– 02

Course Learning Objectives: This course will enable students to

- Simulate discrete time signals and verification of samplingtheorem.
- ComputetheDFTforadiscretesignalandverificationofitspropertiesusingMATLAB.
- Find solution to the difference equations and computation of convolution and correlation along with the verification ofproperties.

1. Computeanddisplaythefilteringoperationsandcomparewiththetheoreticalvalues.
2. Implement the DSP computations on DSP hardware and verify theresult.

Laboratory Experiments

Following Experiments to be done using MATLAB / SCILAB / OCTAVE or equivalent:

1. Verification of sampling theorem (use interpolationfunction).
2. Linear and circular convolution of two given sequences, Commutative, distributive and associative property ofconvolution.
3. Auto and cross correlation of two sequences and verification of theirproperties
4. Solving a given differenceequation.
5. Computation of N point DFT of a given sequence and to plot magnitude and phase spectrum (using DFT equation and verify it by built-inroutine).
6. (i) Verification of DFT properties (like Linearity and Parseval's theorem,etc.)
   (ii) DFT computation of square pulse and Sinc function etc.
7. Design and implementation of Low pass and High pass FIR filter to meet the desired specifications (using different window techniques) and test the filter with an audio file. Plot the spectrum of audio signal before and afterfiltering.
8. Design and implementation of a digital IIR filter (Low pass and High pass) to meet given specificationsandtestwithanaudiofile.Plotthespectrumofaudiosignalbeforeandafterfiltering.

Following Experiments to be done using DSP kit

9. Obtain the Linear convolution of twosequences.
10. Compute Circular convolution of twosequences.
11. Compute the N-point DFT of a givensequence.
12. Determine the Impulse response of first order and second ordersystem.
13. Generation of Sine wave and standard testsignals

Course Outcomes: On the completion of this laboratory course, the students will be able to:

- Apply sampling theorem and effective reconstruction of signal.
- Compute the DFT for a discrete signal and verification of its properties using MATLAB.
- Solve difference equations and perform different operations on discrete time signals
- Design IIR and FIR filters for the given specifications.
- Build DSP computations on TMS processor and verify the result

Conduct of Practical Examination:

1. All laboratory experiments are to be included for practicalexamination.
2. Strictlyfollowtheinstructionsasprintedonthecoverpageofanswerscriptforbreakupofmarks.
3. ChangeofexperimentisallowedonlyonceandMarksallottedtotheprocedureparttobemadezero.

Reference Books:

1. Vinay K Ingle, John G Proakis, Digital Signal Processing using MATLAB, Fourth Edition, Cengage India Private Limited, 2017.

B. E. (EC / TC)
ChoiceBasedCreditSystem(CBCS)andOutcomeBasedEducation(OBE) SEMESTER – V

HDL LABORATORY

Laboratory Code	**18ECL58**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**02Hr Tutorial (Instructions)+ 02 Hours Laboratory**	**SEE Marks**	**60**
RBT Level	**L1, L2, L3**	**Exam Hours**	**03**

CREDITS – 02

Course Learning Objectives: This course will enable students to:

- Familiarize with the CAD tool to write HDLprograms.
- Understand simulation and synthesis of digitaldesign.
- Program FPGAs/CPLDs to synthesize the digitaldesigns.
- Interface hardware to programmable ICs through I/Oports.
- Choose either Verilog or VHDL for a given Abstractionlevel.

Note: Programming can be done using any compiler. Download the programs on a FPGA/CPLD board and performance testing may be done using 32 channel pattern generator and logic analyzer apart from verification by simulation with tools such as Altera/Modelsim or equivalent.

Laboratory Experiments

PART A : Programming

1. WriteVerilogprogramforthefollowingcombinationaldesignalongwithtestbenchtoverifythedesign:
   a. 2to4decoderrealizationusingNANDgatesonly(structuralmodel)
   b. 8to3encoderwithpriorityandwithoutpriority(behaviouralmodel)
   c. 8 to 1 multiplexer using case statement and ifstatements
   d. 4-bitbinarytograyconverterusing1-bitgraytobinaryconverter1-bitadderandsubtractor

2. Model in Verilog for a full adder and addfunctionality to perform logical operations of XOR, XNOR, AND and OR gates. Write test bench with appropriate input patterns to verify the modeled behaviour.

3. Verilog32-bitALU shownin figurebelowandverifythefunctionalityofALUbyselectingappropriate test patterns. The functionality of the ALU is presented in Table1.
   a. WritetestbenchtoverifythefunctionalityoftheALUconsideringallpossibleinputpatterns
   b. The enable signal will set the output to required functions if enabled, if disabled all the outputs are set totri-state
   c. The acknowledge signal is set high after every operation iscompleted

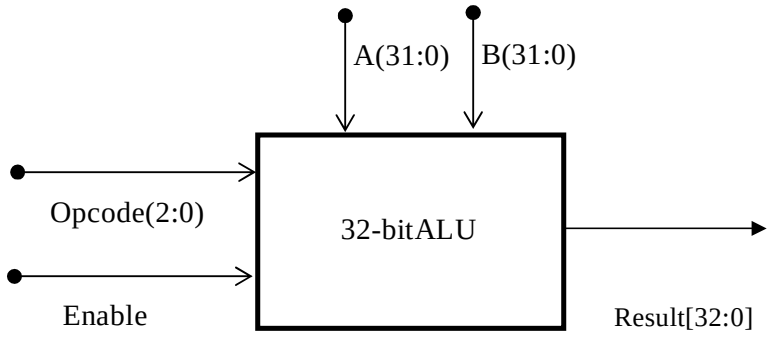

Figure 1 ALU top level block diagram

Opcode(2:0)	ALU Operation	Remarks	
000	A + B	Addition of two numbers	Both A and B are in two's complement format
001	A – B	Subtraction of two numbers	
010	A + 1	Increment Accumulator by 1	A is in two's complement format
011	A - 1	Decrement accumulator by 1	
100	A	True	Inputs can be in any format
101	A Complement	Complement	
110	A OR B	Logical OR	
111	A AND B	Logical AND	

Table 1 ALU Functions

4. Write Verilog code for SR, D and JK and verify the flip flop.

5. Write Verilog code for 4-bit BCD synchronous counter.

6. Write Verilog code for counter with given input clock and check whether it works asclock divider performing division of clock by 2, 4, 8 and 16. Verify the functionality of the code.

PART-B:InterfacingandDebugging(EDWinXP,PSpice,MultiSim,Proteus,CircuitLaboranyother equivalent tool can beused)

1. Write a Verilog code to design a clock divider circuit that generates 1/2, 1/3rd and 1/4thclock from a giveninputclock.PortthedesigntoFPGAandvalidatethefunctionalitythroughoscilloscope.

2. Interface a DC motor to FPGA and write Verilog code to change its speed and direction.

3. Interface a Stepper motor to FPGA and write Verilog code to control the Stepper motor rotation which in turn may control a Robotic Arm. External switches to be used for different controls like rotate the Stepper motor (i) +N steps if Switch no.1 of a Dip switch is closed (ii) +N/2 steps if Switch no. 2 of a Dip switch is closed (iii) –N steps if Switch no. 3 of a Dip switch is closed etc.

4. Interface a DAC to FPGA and write Verilog code to generate Sine wave of frequency F KHz (eg. 200 KHz) frequency. Modify the code to down sample the frequency to F/2 KHz. Display the Original and Down sampled signals by connecting them to an oscilloscope.

5. Write Verilog code using FSM to simulate elevator operation.

6. Write Verilog code to convert an analog input of a sensor to digital form and to display the same on a suitable display like set of simple LEDs, 7-segment display digits or LCD display.

Course Outcomes: At the end of this course, students should be able to:

- Develop and Write the Verilog/VHDL programs to simulate Combinational circuits in Dataflow, Behavioral and Gate level Abstractions
- Develop and Describe sequential circuits like flip flops and counters in Behavioral description and obtain simulation waveforms
- Develop andSynthesize Combinational and Sequential circuits on programmable ICs and test the hardware
- Develop andInterface the hardware to the programmable chips and obtain the required output
- Develop HARDWARE DESCRIPTIVE PROGRAMMES USING Verilog or VHDL for a given Abstraction level

Conduct of Practical Examination:

- All laboratory experiments are to be included for practicalexamination.
- Students are allowed to pick one experiment from thelot.
- Strictlyfollowtheinstructionsasprintedonthecoverpageofanswerscriptforbreakupofmarks.
- ChangeofexperimentisallowedonlyonceandMarksallottedtotheprocedureparttobemadezero.

B. E. Common to all Branches
ChoiceBasedCreditSystem(CBCS)andOutcomeBasedEducation(OBE) SEMESTER – V

ENVIRONMENTAL STUDIES

Course Code	**18CIV59**	**CIE Marks**	**40**
Teaching Hours / Week (L:T:P)	**(1:0:0)**	**SEE Marks**	**60**
Credits	**01**	**Exam Hours**	**02**

Module - 1

Ecosystems (Structure and Function): Forest, Desert, Wetlands, Riverine, Oceanic and Lake.
Biodiversity: Types, Value; Hot-spots; Threats and Conservation of biodiversity, Forest Wealth, and Deforestation.

Module - 2

Advances in Energy Systems (Merits, Demerits, Global Status and Applications)**:** Hydrogen, Solar, OTEC, Tidal and Wind.
Natural Resource Management (Concept and case-studies): Disaster Management, Sustainable Mining, Cloud Seeding, and Carbon Trading.

Module - 3

Environmental Pollution (Sources, Impacts, Corrective and Preventive measures, Relevant Environmental Acts, Case-studies)**:** Surface and Ground Water Pollution; Noise pollution; Soil Pollution and Air Pollution.
Waste Management & Public Health Aspects: Bio-medical Wastes; Solid waste; Hazardous wastes; E-wastes; Industrial and Municipal Sludge.

Module - 4

Global Environmental Concerns(Concept, policies and case-studies):Ground water depletion/recharging, Climate Change; Acid Rain; Ozone Depletion; Radon and Fluoride problem in drinking water; Resettlement and rehabilitation of people, Environmental Toxicology.

Module - 5

Latest Developments in Environmental Pollution Mitigation Tools (Concept and Applications): G.I.S. & Remote Sensing, Environment Impact Assessment, Environmental Management Systems, ISO14001; Environmental Stewardship- NGOs.
Field work: Visit to an Environmental Engineering Laboratory or Green Building or Water Treatment Plant or Waste water treatment Plant; ought to be Followed by understanding of process and its brief documentation.

Course outcomes: At the end of the course, students will be able to:

- Understand the principles of ecology and environmental issues that apply to air, land, and water issues on a globalscale,
- Develop critical thinking and/or observation skills, and apply themtothe analysis of a problem or question related to theenvironment.
- Demonstrateecologyknowledgeofacomplexrelationshipbetweenbioticandabioticcomponents.
- Apply their ecological knowledge to illustrate and graph a problem and describe the realities that managers face when dealing with complexissues.

Question paper pattern:

- The Question paper will have 100 objectivequestions.
- Each question will be for 01marks
- Student will have to answer all the questions in an OMRSheet.
- The Duration of Exam will be 2hours.

Sl. No.	Title of the Book	Name of the Author/s	Name of the Publisher	Edition and Year
		Textbook/s		
1	Environmental Studies	Benny Joseph	Tata McGraw – Hill.	2nd Edition, 2012
2	Environmental Studies	S M Prakash	PristinePublishing House,Mangalore	3rd Edition, 2018
3	Environmental Studies – From Crisis to Cure	R Rajagopalan	Oxford Publisher	2005
		Reference Books		
1	Principals of	Raman Sivakumar	Cengage learning,	2nd Edition, 2005

	Environmental Science and Engineering		Singapur.	
2	Environmental Science – working with the Earth	G.Tyler Miller Jr.	Thomson Brooks /Cole,	11th Edition, 2006
3	Text Book of Environmental and Ecology	Pratiba Sing, AnoopSingh&Piyush Malaviya	Acme Learning Pvt. Ltd. New Delhi.	1st Edition

K.S.INSTITUTE OF TECHNOLOGY, BANGALORE

(AFFLIATED TO VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELGAUM)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGG.

COMPUTER NETWORKS -VII

Course Title: Computer Networks | **Course Code : 18EC71**
Credits:03 | **L-T-P :4-0-0**
Contact Hours/Week: 04 | **Total Hours:50**
Exam. Marks:100 | **IA Marks :30**
Exam. Hours : 03

Course Learning Objectives: This course will enable students to:

- UnderstandthelayeringarchitectureofOSIreferencemodelandTCP/IPprotocolsuite.
- Understand the protocols associated with eachlayer.
- Learn the different networking architectures and theirrepresentations.
- Learn the functions and services associated with eachlayer.

Module-1	RBT Level
Introduction: Data communication: Components, Data representation, Data flow, Networks: Network criteria, Physical Structures, Network types: LAN, WAN, Switching, The Internet. **(1.1,1.2, 1.3(1.3.1to 1.3.4 of Text).** **Network Models:** Protocol Layering: Scenarios, Principles, Logical Connections, TCP/IP ProtocolSuite:LayeredArchitecture,LayersinTCP/IPsuite,Descriptionoflayers,Encapsulation and Decapsulation, Addressing, Multiplexing and Demultiplexing, The OSI Model: OSI Versus TCP/IP. **(2.1, 2.2, 2.3 ofText)**	**L1, L2**
Module-2	
Data-Link Layer: Introduction: Nodes and Links, Services, Two Categories' of link, Sublayers, Link Layer addressing: Types of addresses, ARP. Data Link Control (DLC) services: Framing, Flow and Error Control, Data Link Layer Protocols: Simple Protocol, Stop and Wait protocol, Piggybacking. **(9.1, 9.2(9.2.1, 9.2.2), 11.1, 11.2of Text)** **Media Access Control:** Random Access: ALOHA, CSMA, CSMA/CD, CSMA/CA.**(12.1 of Text).** **WiredandWirelessLANs:**EthernetProtocol,StandardEthernet.IntroductiontowirelessLAN: Architectural Comparison, Characteristics, Access Control**. (13.1, 13.2(13.2.1 to 13.2.5), 15.1 of Text)**	**L1,L2, L3**
Module-3	
Network Layer: Introduction, Network Layer services: Packetizing, Routing and Forwarding, Other services, Packet Switching: Datagram Approach, Virtual Circuit Approach, IPV4 Addresses: Address Space, Classful Addressing, Classless Addressing, DHCP, Network Address Resolution, Forwarding of IP Packets: Based on destination Address and Label. **(18.1, 18.2, 18.4, 18.5.1, 18.5.2 of Text)** **Network Layer Protocols:** Internet Protocol (IP): Datagram Format, Fragmentation, Options, Security of IPv4 Datagrams. **(19.1of Text)**. **Unicast Routing:** Introduction, Routing Algorithms: Distance Vector Routing, Link State Routing, Path vector routing. **(20.1, 20.2of Text)**	**L1,L2, L3**
Module-4	

Transport Layer: Introduction: Transport Layer Services, Connectionless and Connection orientedProtocols,TransportLayerProtocols:Simpleprotocol,Stopandwaitprotocol,Go-Back-NProtocol,Selectiverepeatprotocol.**(23.1,23.2.1,23.2.2,23.2.3,23.2.4ofText)** **Transport-Layer Protocols in the Internet:** UserDatagramProtocol:UserDatagram,UDPServices,UDPApplications,TransmissionControl	**L1,L2, L3**
Protocol: TCP Services, TCP Features, Segment, Connection, State Transition diagram, Windows in TCP, Flow control, Error control, TCP congestion control. **(24.2, 24.3.1, 24.3.2, 24.3.3, 24.3.4, 24.3.5, 24.3.6, 24.3.7, 24.3.8, 24.3.9 of Text)**	
Module-5	
Application Layer: Introduction: providing services, Application- layer paradigms, Standard Client–ServerProtocols:Worldwideweb,HyperTextTransferProtocol,FTP:Twoconnections, Control Connection, Data Connection, Electronic Mail: Architecture, Wed Based Mail, Telnet: Local versus remote logging.Domain Name system: Name space, DNS in internet, Resolution, DNSMessages,Registrars,DDNS,securityofDNS.**(25.1,26.1,26.2,26.3,26.4,26.6ofText)**	**L1, L2**

Course Outcomes: At the end of the course, the students will be able to:

- Make use of the layering architecture of computer networks and distinguish between the OSI reference model and TCP/IP protocol suite.
- Identify the protocols and services of Data link layer and Media access control.
- Distinguish wired and wireless LANS architectures, protocols and the associated connecting devices.
- Analyse the packetizing, routing and forwarding services and associated protocols of Network layer.
- Analyse the protocols and functions associated with the transport layer services.

Question paper pattern:

- Examinationwillbeconductedfor100markswithquestionpapercontaining10fullquestions,eachof20 marks.
- Each full question can have a maximum of 4 subquestions.
- Therewillbe2fullquestionsfromeachmodulecoveringallthetopicsofthemodule.
- Studentswillhavetoanswer5fullquestions,selectingonefullquestionfromeachmodule.
- Thetotalmarkswillbeproportionallyreduced to60 marksasSEEmarksis60.

TEXTBOOK:

Forouzan, “Data Communications and Networking” , 5th Edition, McGraw Hill, 2013, ISBN: 1-25-906475-3.

REFERENCE BOOKS:

1. James J Kurose, Keith W Ross, Computer Networks, , PearsonEducation.
2. WayarlesTomasi,IntroductiontoDataCommunicationandNetworking,PearsonEducation.
3. Andrew Tanenbaum, “Computer networks”, PrenticeHall.
4. William Stallings, “Data and computer communications”, PrenticeHall,

B. E. ECE
ChoiceBasedCreditSystem(CBCS)andOutcomeBasedEducation(OBE) SEMESTER – VII

VLSI DESIGN

Course Code	**18EC72**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of LectureHours	**40 (08 Hours / Module)**	**Exam Hours**	**03**

CREDITS – 03

Course Learning Objectives: The objectives of the course is to enable students to:

- Impart knowledge of MOS transistor theory and CMOStechnologies
- Learn the operation principles and analysis of invertercircuits.
- DesignCombinational,sequentialanddynamiclogiccircuitsaspertherequirements
- Infer the operation of Semiconductors Memorycircuits.
- Demonstrate the concepts of CMOStesting

Module-1	**RBT Level**
Introduction: A Brief History, MOS Transistors, CMOS Logic **(1.1 to 1.4 of TEXT2)** **MOS Transistor Theory:** Introduction, Long-channel I-V Characteristics, Non-ideal I-V Effects, DC Transfer Characteristics **(2.1, 2.2, 2.4 and 2.5 of TEXT2).**	**L1, L2**
Module-2	
Fabrication: CMOS Fabrication and Layout, VLSI Design Flow, Introduction, CMOS Technologies, Layout Design Rules, **(1.5 and 3.1 to 3.3 of TEXT2).** MOSFET Scaling and Small-Geometry Effects, MOSFET Capacitances **(3.5 to 3.6 of TEXT1)**	**L1, L2,**
Module-3	
Delay: Introduction, Transient Response, RC Delay Model, Linear Delay Model, Logical Efforts of Paths **(4.1 to 4.5 of TEXT2, except sub-sections 4.3.7, 4.4.5, 4.4.6, 4.5.5 and 4.5.6).** **Combinational Circuit Design:** Introduction, Circuit families **(9.1 to 9.2 of TEXT2, except subsection 9.2.4).**	**L1, L2, L3**
Module-4	
Sequential Circuit Design: Introduction, Circuit Design for Latches and Flip-Flops **(10.1 and 10.3.1 to 10.3.4 of TEXT2)** **Dynamic Logic Circuits:** Introduction, Basic Principles of Pass Transistor Circuits, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques **(9.1, 9.2, 9.4 to 9.5 of TEXT1)**	**L1, L2, L3**
Module-5	
Semiconductor Memories: Introduction, Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM), **(10.1 to 10.3 of TEXT1)** **Testing and Verification:** Introduction, Logic Verification Principles, Manufacturing Test Principles, Design for testability **(15.1, 15.3, 15.5 15.6.1 to 15.6.3 of TEXT 2).**	**L1, L2**

Course outcomes: At the end of the course, the students will be able to:

- Utilize the concept of basic MOS transistor, CMOS fabrication flow and technology scaling.
- Make use of the knowledge of physical design aspects to make stick and layout diagrams for various gates.
- Identify the concept of Memory elements along with timing considerations with scaling fundamentals
- Experiment with the basic knowledge of FPGA based system design and testability issues in VLSI Design
- Analyze the various CMOS subsystems and architectural issues with the design constraints.

Question paper pattern:

- Examinationwillbeconductedfor100markswithquestionpapercontaining10fullquestions,eachof20 marks.
- Each full question can have a maximum of 4 subquestions.
- Therewillbe2fullquestionsfromeachmodulecoveringallthetopicsofthemodule.
- Studentswillhavetoanswer5fullquestions,selectingonefullquestionfromeachmodule.
- Thetotalmarkswillbeproportionallyreduced to60 marksasSEEmarksis60.

TEXT BOOKS:

1. "CMOSDigitalIntegratedCircuits:AnalysisandDesign"-
SungMoKang&YosufLeblebici, Third Edition, TataMcGraw-Hill.

2. "CMOSVLSIDesign-ACircuitsandSystemsPerspective"-NeilH.E.Weste, and
David Money Harris4th Edition, PearsonEducation.

REFERENCE BOOKS:

1. AdelSedraandK.C.Smith,"MicroelectronicsCircuitsTheoryandApplications",6th or 7th Edition, Oxford University Press, International Version,2009.
2. DouglasAPucknell&KamranEshragian,"BasicVLSIDesign",PHI3rdEdition,(originalEdition – 1994).
3. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", TMH,2007.

Professional Elective – 2

B. E. (EC/TC)
ChoiceBasedCreditSystem(CBCS)andOutcomeBasedEducation(OBE) SEMESTER – VII

REAL TIME SYSTEM

Course Code	**18EC731**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (08 Hours per Module)**	**Exam Hours**	**03**

Credits – 03

Course Learning Objectives: This Course will enable students to:

- Understand the fundamentals of Real-time systems and itsclassifications.
- Describetheconceptsofcomputercontrolandhardwarecomponentsfor Real-TimeApplication.
- Discuss the languages to develop software for Real-TimeApplications.
- Explain the concepts of operating system and RTS developmentmethodologies.

Module-1	RBT Levels
Introduction to Real-Time Systems: Historical background, Elements of a Computer Control System,RTS-Definition,ClassificationofReal-timeSystems,TimeConstraints,Classificationof Programs. **Concepts of Computer Control:** Introduction, Sequence Control, Loop Control, Supervisory Control, Centralized Computer Control, Hierarchical Systems. **(Text: 1.1 to 1.6 and 2.1 to 2.6)**	**L1, L2**
Module-2	
Computer Hardware Requirements for Real-Time Applications: Introduction, General Purpose Computer, Single Chip Microcomputers and Microcontrollers, Specialized Processors, Process-Related Interfaces, Data Transfer Techniques, Communications, Standard Interface. **(Text: 3.1 to 3.8).**	**L1, L2**
Module-3	
Languages for Real-Time Applications: Introduction, Syntax Layout and Readability, Declaration and Initialization of Variables and Constants, Cutlass, Modularity and Variables, Compilation of Modular Programs, Data types, Control Structures, Exception Handling, Low-level facilities, Co-routines, Interrupts and Device Handling, Concurrency, Real-Time Support, Overview of Real-Time Languages. **(Text: 5.1 to 5.14).**	**L1,L2, L3**
Module-4	
Operating Systems: Introduction, Real-Time Multi-Tasking OS, Scheduling Strategies, Priority Structures, Task Management, Scheduler and Real-Time Clock Interrupt Handler, Memory Management, Code Sharing, Resource Control, Task Co-Operation and Communication, Mutual Exclusion.**(Text: 6.1 to 6.11).**	**L1, L2**
Module-5	
Design of RTS – General Introduction: Introduction, Specification Document, Preliminary Design, Single-Program Approach, Foreground/Background System. **RTS Development Methodologies:** Introduction, Yourdon Methodology, Ward and Mellor Method, Hately and Pirbhai Method. **(Text: 7.1 to 7.5 and 8.1, 8.2, 8.4,8.5).**	**L1, L2, L3**

Course Outcomes: At the end of the course, students should be able to:

- Explain the fundamentals of Real time systems and itsclassifications.
- Understand the concepts of computer control and the suitable computer hardware requirements for real-timeapplications.
- Describetheoperatingsystemconceptsandtechniquesrequiredforrealtimesystems.
- Developthesoftwarealgorithmsusingsuitablelanguagestomeet Realtimeapplications.
- Apply suitable methodologies to design and develop Real-TimeSystems.

Text Book:

Real-Time Computer Control, by Stuart Bennet, 2nd Edn. Pearson Education. 2008.

Reference Books:

1. C.M.Krishna,KangG.Shin,“Real–TimeSystems”,McGraw–HillInternationalEditions,1997.
2. Real-TimeSystemsDesignandAnalysis,Phillip.A.Laplante,secondedition,PHI,2005.
3. Embedded Systems, Raj Kamal, Tata McGraw Hill, India, third edition,2005.

B. E. (EC/TC)
ChoiceBasedCreditSystem(CBCS)andOutcomeBasedEducation(OBE) SEMESTER – VII

SATELLITE COMMUNICATION

Course Code	**18EC732**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of LectureHours	**40 (8 Hours / Module)**	**Exam Hours**	**03**

CREDITS – 03

Course Learning Objectives: This course will enable students to

- Understand the basic principle of satellite orbits andtrajectories.
- Study of electronic systems associated with a satellite and the earthstation.
- Understand the various technologies associated with the satellitecommunication.
- Focus on a communication satellite and the national satellitesystem.
- Study of satellite applications focusing various domains services such as remote sensing, weather forecasting andnavigation.

Module-1	**RBT Level**
Satellite Orbits and Trajectories: Definition, Basic Principles, Orbital parameters, Injection velocity and satellite trajectory, Types of Satellite orbits, Orbital perturbations, Satellite stabilization, Orbital effects on satellite's performance, Eclipses, Look angles: Azimuth angle, Elevation angle.	**L1, L2**
Module-2	
Satellite subsystem: Power supply subsystem, Attitude and Orbit control, Tracking, Telemetry and command subsystem, Payload. **Earth Station:** Types of earth station, Architecture, Design considerations, Testing, Earth station Hardware, Satellite tracking.	**L1, L2**
Module-3	
Multiple Access Techniques: Introduction, FDMA (No derivation), SCPC Systems, MCPC Systems, TDMA, CDMA, SDMA. **Satellite Link Design Fundamentals**: Transmission Equation, Satellite Link Parameters, Propagation considerations	**L1,L2, L3**
Module-4	
Communication Satellites: Introduction, Related Applications, Frequency Bands, Payloads, Satellite Vs. Terrestrial Networks, Satellite Telephony, Satellite Television, Satellite radio, Regional satellite Systems, National Satellite Systems.	**L1, L2**
Module-5	
Remote Sensing Satellites: Classification of remote sensing systems, orbits, Payloads, Types of images: Image Classification, Interpretation, Applications. **Weather Forecasting Satellites**: Fundamentals, Images, Orbits, Payloads, Applications. **Navigation Satellites**: Development of Satellite Navigation Systems, GPS system, Applications.	**L1,L2, L3**

Course Outcomes: At the end of the course, the students will be able to:

- Describethesatelliteorbitsanditstrajectorieswiththedefinitionsofparametersassociatedwithit.
- Describetheelectronichardwaresystemsassociatedwiththesatellitesubsystemandearthstation.
- Describethevariousapplicationsofsatellitewiththefocusonnationalsatellitesystem.
- Computethesatellitelinkparametersundervariouspropagationconditionswiththeillustrationofmultiple accesstechniques.

Question paperpattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20marks.
- Each full question can have a maximum of 4 subquestions.
- Therewillbe2fullquestionsfromeachmodulecoveringallthetopicsofthemodule.
- Studentswillhavetoanswer5fullquestions,selectingonefullquestionfromeachmodule.
- Thetotalmarkswillbeproportionallyreduced to60 marksasSEEmarksis60.

Text Book:

Anil K. Maini, Varsha Agrawal, Satellite Communications, Wiley India Pvt. Ltd., 2015, ISBN: 978-81-265-2071-8.

Reference Books :

1. Dennis Roddy, Satellite Communications, 4th Edition, McGraw- Hill International edition,2006
2. TimothyPratt,CharlesBostian,JeremyAllnutt,SatelliteCommunications,2nd Edition,WileyIndiaPvt. Ltd , 2017, ISBN:978-81-265-0833-4

B. E. (EC/TC)
ChoiceBasedCreditSystem(CBCS)andOutcomeBasedEducation(OBE) SEMESTER – VII

DIGITAL IMAGEPROCESSING

Course Code	**18EC733**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40(08HoursperModule)**	**Exam Hours**	**03**

CREDITS– 03

Course Learning Objectives: This course will enable students to

- Understand the fundamentals of digital imageprocessing.
- Understand the image transforms used in digital imageprocessing.
- Understand the image enhancement techniques used in digital imageprocessing.
- Understandtheimagerestoration techniquesandmethodsusedindigitalimageprocessing.
- Understand the Morphological Operations used in digital imageprocessing.

Module1	**RBT Level**
Digital Image Fundamentals: Whatis Digital Image Processing?, Origins of Digital Image Processing, Examples of fields that use DIP, Fundamental Steps in Digital Image Processing, ComponentsofanImageProcessingSystem,ElementsofVisualPerception,ImageSensingand Acquisition. **(Text:Chapter1andChapter2:Sections2.1to2.2,2.6.2)**	**L1,L2**
Module-2	
ImageEnhancementintheSpatialDomain:ImageSamplingandQuantization, Some Basic Relationships Between Pixels, Linear and Nonlinear Operations. Some Basic Intensity Transformation Functions, Histogram Processing, Fundamentals of SpatialFiltering, Smoothing Spatial Filters, Sharpening Spatial Filters **(Text:Chapter2:Sections 2.3to2.62,Chapter3:Sections3.2to3.6)**	**L1,L2**
Module-3	
FrequencyDomain: PreliminaryConcepts, The Discrete Fourier Transform (DFT)ofTwoVariables,Propertiesofthe2-DDFT,Filteringinthe FrequencyDomain,ImageSmoothingandImageSharpeningUsingFrequencyDomainFilters,SelectiveFiltering. **(Text:Chapter4: Sections4.2, 4.5to 4.10)**	**L1,L2**
Module-4	
Restoration:Noisemodels,RestorationinthePresenceofNoiseOnlyusingSpatialFilteringandFrequencyDomainFiltering,Linear,Position-Invariantdegradations,EstimatingtheDegradationFunction,InverseFiltering,MinimumMeanSquareError(Wiener)Filtering,ConstrainedLeastSquares Filtering. **(Text:Chapter5:Sections5.2,to5.9)**	**L1,L2**
Module-5	
Morphological Image Processing: Preliminaries, Erosion and Dilation, Opening and Closing. Color Image Processing: Color Fundamentals, Color Models, Pseudo color Image Processing. **(Text: Chapter 6: Sections 6.1 to 6.3 Chapter 9: Sections9.1to9.3)**	**L1,L2**

Course Outcomes: At the end of the course, students should be able to:

- Understandimageformationandtherolehumanvisualsystemplaysinperceptionofgrayandcolorimage data.
- Applyimageprocessingtechniques inboththespatialandfrequency(Fourier)domains.
- Design and evaluate image analysistechniques
- ConductindependentstudyandanalysisofImageEnhancementandrestoration techniques.

Question paper pattern:

- Examinationwillbeconductedfor100markswithquestionpapercontaining10fullquestions,eachof20 marks.
- Eachfullquestioncanhaveamaximumof4subquestions.
- Therewillbe2fullquestionsfromeach modulecoveringallthetopicsofthemodule.
- Studentswillhavetoanswer5fullquestions,selectingonefullquestionfromeachmodule.
- Thetotalmarkswillbeproportionallyreduced to60marksasSEEmarksis60.

Text Book:

DigitalImageProcessing-RafelCGonzalezandRichardE.Woods,PHI3rd Edition 2010.

Reference Books:

1. DigitalImageProcessing-S.Jayaraman,S.Esakkirajan,T.Veerakumar,TataMcGrawHill2014.
2. FundamentalsofDigitalImageProcessing-A.K.Jain,Pearson2004.
3. ImageProcessinganalysisandMachinevisionwithMindTapbyMilanSonkaandRogerBoile,Cengage Publications,2018.

B. E. ECE
ChoiceBasedCreditSystem(CBCS)andOutcomeBasedEducation(OBE) SEMESTER – VII

DSP ALGORITHMS andARCHITECTURE

Course Code	**18EC734**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**Exam Marks**	**60**
Total Number of Lecture Hours	**40 (08 Hours per Module)**	**Exam Hours**	**03**

CREDITS – 03

Course Learning Objectives: This course will enable students to:

- Figure out the knowledge and concepts of digital signal processingtechniques.
- UnderstandthecomputationalbuildingblocksofDSPprocessorsanditsspeedissues.
- Understand the various addressing modes, peripherals, interrupts and pipelining structure of TMS320C54xx processor.
- LearnhowtointerfacetheexternaldevicestoTMS320C54xxprocessorin variousmodes.
- Understand basic DSP algorithms with theirimplementation.

Module -1	**RBT Level**
Introduction to Digital Signal Processing: Introduction, A Digital Signal – Processing System, The Sampling Process, Discrete Time Sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear Time-Invariant Systems, Digital Filters, Decimation and Interpolation. **Computational Accuracy in DSP Implementations:** NumberFormatsforSignalsandCoefficientsinDSPSystems,DynamicRangeandPrecision,Sourcesof Error in DSPImplementation.	**L1,L2**
Module -2	
Architectures for Programmable Digital Signal – Processing Devices: Introduction, Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External Interfacing.	**L1,L2**
Module -3	
Programmable Digital Signal Processors: Introduction, Commercial Digital Signal-processing Devices, Data Addressing Modes of TMS32OC54XX, Memory Space of TMS32OC54xx Processors, Program Control. Detail Study of TMS320C54X & 54xx Instructions and Programming, On – Chip Peripherals, Interrupts of TMS32OC54XX Processors, Pipeline Operation of TMS32OC54xx Processor.	**L1,L2**
Module -4	
Implementation of Basic DSP Algorithms: Introduction, The Q – notation, FIR Filters, IIR Filters, Interpolation and Decimation Filters (one example in each case). **Implementation of FFT Algorithms:** Introduction, An FFT Algorithm for DFT Computation, Overflow and Scaling, Bit – Reversed Index. Generation & Implementation on the TMS32OC54xx.	**L1,L2**
Module-5	
Interfacing Memory and Parallel I/O Peripherals to Programmable DSP Devices: Introduction, Memory Space Organization, External Bus Interfacing Signals. Memory Interface, Parallel I/O Interface, Programmed I/O, Interrupts and I/O Direct Memory Access (DMA). **Interfacing and Applications of DSP Processors:** Introduction, Synchronous Serial Interface, A CODEC Interface Circuit, DSP Based Bio-telemetry Receiver, A Speech Processing System, An Image Processing System.	**L1,L2**

Course Outcomes: At the end of this course, students would be able to

- Comprehend the knowledge and concepts of digital signal processingtechniques.
- ApplytheknowledgeofDSPcomputationalbuildingblockstoachievespeedinDSParchitectureorprocessor.
- Apply knowledge of various types of addressing modes, interrupts, peripherals and pipelining structure of TMS320C54xxprocessor.
- Develop basic DSP algorithms using DSPprocessors.
- Discussaboutsynchronousserialinterfaceandmultichannelbufferedserialport(McBSP)ofDSPdevice.
- Demonstrate the programming of CODECinterfacing.

Question paper pattern:

- Examinationwillbeconductedfor100markswithquestionpapercontaining10fullquestions,eachof20marks.
- Each full question can have a maximum of 4 subquestions.
- Therewillbe2fullquestionsfromeachmodulecoveringallthetopicsofthe module.
- Studentswillhave toanswer5fullquestions,selectingonefullquestionfromeachmodule.
- Thetotalmarkswillbeproportionallyreduced to60 marksas SEEmarksis60.

Text Book:

"Digital Signal Processing", Avatar Singh and S. Srinivasan, Thomson Learning, 2004.

Reference Books:

1. "DigitalSignalProcessing:Apracticalapproach",IfeachorE.C.,JervisB.WPearson-Education,PHI,2002.
2. "Digital Signal Processors", B Venkataramani and M Bhaskar, TMH, 2nd,2010
3. "Architectures for Digital Signal Processing", Peter Pirsch John Wiley,2008

Professional Electives – 3

B. E. (EC/TC) ChoiceBasedCreditSystem(CBCS)andOutcomeBasedEducation(OBE) SEMESTER – VII			
IoT & WIRELESS SENSOR NETWORKS			
Course Code	**18EC741**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of LectureHours	**40 (8 Hours / Module)**	**Exam Hours**	**03**
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Describe the OSI Model for IoT/M2MSystems.
- Understand the architecture and design principles for device supportingIoT.
- Develop competence in programming for IoTApplications.
- Identifytheuplinkanddownlinkcommunicationprotocolswhichbestsuitsthe specific application of IOT /WSNs.

Module-1	RBT Levels
Overview of Internet of Things: IoT Conceptual Framework, IoT Architectural View, Technology Behind IoT, Sources of IoT,M2M communication, Examples of IoT. Modified OSI ModelfortheIoT/M2MSystems,dataenrichment,dataconsolidationanddevicemanagementat IoT/M2M Gateway, web communication protocols used by connected IoT/M2M devices, Message communication protocols (CoAP-SMS, CoAP-MQ, MQTT,XMPP) for IoT/M2M devices. – Refer Chapter 1, 2 and 3 of Text1.	**L1, L2**
Module-2	
Architecture and Design Principles for IoT: Internet connectivity, Internet-based communication,IPv4, IPv6,6LoWPAN protocol, IP Addressing in the IoT, Application layer protocols: HTTP, HTTPS,FTP,TELNET and ports. **Data Collection, Storage and Computing using a Cloud Platform:** Introduction, Cloud computing paradigm for data collection, storage and computing, Cloud service models, IoT Cloud- based data collection, storage and computing services using Nimbits. - Refer Chapter 4 and 6 of Text 1.	**L1, L2**
Module-3	
Prototyping and Designing Software for IoT Applications: Introduction, Prototyping Embedded device software, Programming Embedded Device Arduino Platform using IDE, Reading data from sensors and devices, Devices, Gateways, Internet and Web/Cloud services software development. Programming MQTT clients and MQTT server. Introduction to IoT privacy and security. Vulnerabilities, security requirements and threat analysis, IoT Security Tomography and layered attacker model. - Refer Chapter 9 and 10 of Text 1.	**L1, L2, L3**
Module-4	
Overview of Wireless Sensor Networks: Challenges for Wireless Sensor Networks, Enabling Technologies for Wireless Sensor Networks. **Architectures**: Single-Node Architecture - Hardware Components, Energy Consumption of Sensor Nodes, Operating Systems and Execution Environments, Network Architecture-Sensor Network Scenarios, Optimization Goals and Figures of Merit, Design principles for WSNs, Service interfaces of WSNs Gateway Concepts. - Refer Chapter 1, 2, 3 of Text 2.	**L1, L2, L3**
Module-5	

Communication Protocols: Physical Layer and Transceiver Design Considerations, MAC Protocols for Wireless Sensor Networks, Low Duty Cycle Protocols And Wakeup Concepts - S-MAC , The Mediation Device Protocol,WakeupRadioConcepts,Contentionbasedprotocols(CSMA,PAMAS),Schedulebased protocols (LEACH, SMACS, TRAMA) Address and Name Management in WSNs, Assignment of MAC Addresses, Routing Protocols- Energy-Efficient Routing, Geographic Routing, Hierarchical networksbyclustering. -ReferChapter4,5,7and11ofText2.	**L1, L2, L3**

Course Outcomes: At the end of the course, students will be able to:

- Understand choice and application of IoT & M2M communicationprotocols.
- Describe Cloud computing and design principles ofIoT.
- Awareness of MQTT clients, MQTT server and itsprogramming.
- Develop an architecture and its communication protocols of ofWSNs.

Question paper pattern:

- Examinationwillbeconductedfor100markswithquestionpapercontaining10fullquestions,eachof20 marks.
- Eachfullquestioncanhaveamaximumof4subquestions.
- Therewillbe2fullquestionsfromeachmodulecoveringallthetopicsofthemodule.
- Studentswillhavetoanswer5fullquestions,selectingonefullquestionfromeachmodule.
- Thetotalmarkswillbeproportionallyreduced to60marksasSEEmarksis60.

Text Books:

1. RajKamal,"InternetofThings-Architectureanddesignprinciples",McGrawHillEducation.
2. Holger Karl & Andreas Willig, "Protocols And Architectures for Wireless Sensor Networks", John Wiley, 2005.

Reference Books:

1. Feng Zhao & Leonidas J. Guibas, "Wireless Sensor Networks- An Information Processing Approach", Elsevier,2007.
2. Kazem Sohraby, Daniel Minoli, &TaiebZnati, "Wireless Sensor Networks- Technology, Protocols, And Applications", John Wiley,2007.
3. Anna Hac, "Wireless Sensor Network Designs", John Wiley,2003.

B. E. (EC/TC)
ChoiceBasedCreditSystem(CBCS)andOutcomeBasedEducation(OBE) SEMESTER – VII

AUTOMOTIVE ELECTRONICS

Course Code	**18EC742**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**3**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (8Hours/Module)**	**Exam Hours**	**03**

CREDITS – 03

Course Learning Objectives: This course will enable students to:

- Understandthebasicsofautomobiledynamicsanddesignelectronicstocomplementthosefeatures.
- Designandimplementtheelectronicsthatattributethereliability,safety,andsmartnesstothe automobiles, providing add-oncomforts.

Module -1	**RBT Level**
Automotive Fundamentals Overview – Evolution of Automotive Electronics, Automobile Physical Configuration, Survey of Major Automotive Systems, The Engine – Engine Block, Cylinder Head, Four Stroke Cycle, Engine Control, Ignition System - Spark plug, High voltage circuit and distribution, Spark pulse generation, Ignition Timing, Diesel Engine, Drive Train - Transmission, Drive Shaft, Differential, Suspension, Brakes, Steering System (Text 1: Chapter1), Starter Battery –Operating principle: **(Text 2: Pg. 407-410)** **The Basics of Electronic Engine Control –** Motivation for Electronic Engine Control – Exhaust Emissions,FuelEconomy,ConceptofanElectronicEnginecontrolsystem,DefinitionofGeneral terms, Definition of Engine performance terms, Engine mapping, Effect of Air/Fuel ratio, spark timingandEGRonperformance,ControlStrategy,ElectronicFuelcontrolsystem,Analysisof intake manifold pressure, Electronic Ignition. **(Text 1: Chapter 5)**	**L1, L2**
Module -2	
Automotive Sensors – Automotive Control System applications of Sensors and Actuators – Variables to be measured, Airflow rate sensor, Strain Gauge MAP sensor, Engine Crankshaft Angular Position Sensor, Magnetic Reluctance Position Sensor, Hall effect Position Sensor, Shielded Field Sensor, Optical Crankshaft Position Sensor, Throttle Angle Sensor (TAS), Engine Coolant Temperature (ECT) Sensor, Exhaust Gas Oxygen (O2/EGO) Lambda Sensors, Piezoelectric Knock Sensor. **(Text 1: Chapter 6)** **AutomotiveEngineControlActuators–**Solenoid,FuelInjector,EGRActuator,IgnitionSystem **(Text 1: Chapter 6)**	**L1, L2**
Module -3	
DigitalEngineControlSystems–DigitalEnginecontrolfeatures,ControlmodesforfuelControl (Seven Modes), EGR Control, Electronic Ignition Control - Closed loop Ignition timing, Spark Advance Correction Scheme, Integrated Engine Control System - Secondary Air Management, EvaporativeEmissionsCanisterPurge,AutomaticSystemAdjustment,SystemDiagnostics.**(Text 1: Chapter7)** **Control Units –** Operating conditions, Design, Data processing, Programming, Digital modules in the Control unit, Control unit software. **(Text 2: Pg. 196-207)**	**L1, L2**
Module -4	
Automotive Networking –Bus Systems – Classification, Applications in the vehicle, Coupling of networks, Examples of networked vehicles **(Text 2: Pg. 85-91),** Buses - CAN Bus, LIN Bus, MOST Bus, Bluetooth, Flex Ray, Diagnostic Interfaces. **(Text 2: Pg. 92-151)** **Vehicle Motion Control** – Typical Cruise Control System, Digital Cruise Control System, Digital Speed Sensor, Throttle Actuator, Digital Cruise Control configuration, Cruise Control Electronics (Digital only), Antilock Brake System (ABS) **(Text 1: Chapter 8)**	**L1,L2**
Module -5	
Automotive Diagnostics–Timing Light, Engine Analyzer, On-board diagnostics, Off-board diagnostics, Expert Systems, Occupant Protection Systems – Accelerometer based Air Bag systems. **(Text 1: Chapter 10)** **Future AutomotiveElectronic Systems** – Alternative Fuel Engines, Electric and Hybrid vehicles, Fuel cell powered cars, Collision Avoidance Radar warning Systems, Low tirepressure	**L1, L2,L3**

warning system, Heads Up display, Speech Synthesis, Navigation – Navigation Sensors - Radio Navigation, Signpost navigation, dead reckoning navigation, Voice Recognition Cell Phone dialing, Advanced Cruise Control, Stability Augmentation, Automatic driving Control **(Text 1: Chapter 11)**	

Course Outcomes: At the end of the course, students will be able to:

- Acquire an overview of automotive components, subsystems, and basics of Electronic Engine Control in today's automotiveindustry.
- Useavailableautomotivesensorsandactuatorswhileinterfacingwithmicrocontrollers/microprocessors during automotive systemdesign.
- Understand the networking of various modules in automotive systems, communication protocols and diagnostics of the subsystems.
- Design and implement the electronics that attribute the reliability, safety, and smartness to the automobiles,providingadd-oncomfortsandgetfairideaonfutureAutomotiveElectronicSystems.

Question paper pattern:

- Examinationwillbeconductedfor100markswithquestionpapercontaining10fullquestions,eachof20 marks.
- Eachfullquestioncanhaveamaximumof4subquestions.
- Therewillbe2fullquestionsfromeachmodulecoveringallthetopicsofthemodule.
- Studentswillhavetoanswer5fullquestions,selectingonefullquestionfromeachmodule.
- Thetotalmarkswillbeproportionallyreducedto60marksasSEEmarksis60.

Text Books:

1. WilliamB.Ribbens,"UnderstandingAutomotiveElectronics",6thEdition,ElsevierPublishing.
2. Robert Bosch Gmbh (Ed.) Bosch Automotive Electrics and Automotive Electronics Systems and Components,NetworkingandHybridDrive,5thedition,JohnWiley&SonsInc.,2007.

B. E. (EC/TC)
ChoiceBasedCreditSystem(CBCS)andOutcomeBasedEducation(OBE) SEMESTER – VII

MULTIMEDIA COMMUNICATION

Course Code	**18EC743**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**Exam Marks**	**60**
Total Number of Lecture Hours	**40 (08 Hours per Module)**	**Exam Hours**	**03**

CREDITS – 03

Course Learning Objectives: This course will enable students to:

- Understandtheimportanceofmultimediaintoday'sonlineandofflineinformationsourcesand repositories.
- UnderstandthehowText,Audio,ImageandVideoinformationcanberepresenteddigitallyinacomputer so that it can be processed, transmitted and storedefficiently.
- UnderstandtheMultimediaTransportinWirelessNetworks
- UnderstandtheReal-timemultimedianetworkapplications.
- Understand the Different network layer basedapplication.

Module -1	**RBT Level**
Multimedia Communications: Introduction, Multimedia information representation, multimedia networks, multimedia applications, Application and networking terminology. (**Chapter 1 of Text1)**	**L1,L2**
Module -2	
Information Representation: Introduction, Digitization principles, Text, Images, Audio and Video.**(Chapter 2 of Text 1)**	**L1,L2**
Module -3	
Text and Image Compression: Introduction, Compression principles, text compression, image Compression.**(Chapter 3 of Text 1)** **Distributed Multimedia Systems:** Introduction, main Features of a DMS, Resource management of DMS, Networking, Multimedia Operating Systems. **(Chapter 4 - Sections 4.1 to 4.5 of Text 2)**	**L1,L2**
Module -4	
Audio and video compression: Introduction, Audio compression, video compression, video compression principles, video compression.**(Chapter 4 of Text 1)**	**L1,L2**
Module-5	
Multimedia Information Networks: Introduction, LANs, Ethernet, Token ring, Bridges, FDDI High-speed LANs, LAN protocol**(Chap. 8 of Text 1).** **TheInternet:**Introduction,IPDatagrams,Fragmentation,IPAddress,ARPandRARP,QoS Support, IPv8.**(Chap. 9 of Text1)**	**L1,L2**

Course Outcomes: After studying this course, students will be able to:

- Understand basics of different multimedia networks andapplications.
- Understand different compression techniques to compress audio andvideo.
- Describe multimedia Communication acrossNetworks.
- Analyse different media types to represent them in digitalform.
- Compressdifferenttypesoftextandimagesusingdifferentcompressiontechniques.

Question paper pattern:

- Examinationwillbeconductedfor100markswithquestionpapercontaining10fullquestions,eachof20 marks.
- Each full question can have a maximum of 4 subquestions.
- Therewillbe2fullquestionsfromeachmodulecoveringallthetopicsofthemodule.
- Studentswillhavetoanswer5fullquestions,selectingonefullquestionfromeachmodule.
- Thetotalmarkswillbeproportionallyreduced to60 marksasSEEmarksis60.

Text Book:

1. MultimediaCommunications-FredHalsall,PearsonEducation,2001,ISBN-9788131709948.
2. MultimediaCommunicationSystems-K.R.Rao,ZoranS.Bojkovic,DragoradA.Milovanovic,Pearson Education, 2004. ISBN-9788120321458.

Reference Book:

Multimedia:Computing,CommunicationsandApplications-Raifsteinmetz,KlaraNahrstedt,Pearson Education,2002.ISBN-978817758

B. E. (EC/TC)
ChoiceBasedCreditSystem(CBCS)andOutcomeBasedEducation(OBE) SEMESTER – VII

CRYPTOGRAPHY

Course Code	**18EC744**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**Exam Marks**	**60**
Total Number of Lecture Hours	**40 (08 Hours per Module)**	**Exam Hours**	**03**

CREDITS – 03

Course Learning Objectives: This course will enable students to:

- Understand the basics of symmetric key and public keycryptography.
- Explain classical cryptographyalgorithms.
- Acquire knowledge of mathematical concepts required forcryptography.
- Describe pseudo random sequence generationtechnique.
- Explain symmetric and asymmetric cryptographyalgorithms.

Module -1	RBT Level
Classical Encryption Techniques: Symmetric cipher model, Substitution techniques, Transposition techniques **(Text 1: Chapter 1)** **BasicConceptsofNumberTheoryandFiniteFields:**Euclideanalgorithm,Modulararithmetic **(Text 1: Chapter 3)**	**L1,L2**
Module -2	
SYMMETRIC CIPHERS: Traditional Block Cipher structure, Data encryption standard (DES), The AES Cipher. **(Text 1: Chapter 2: Section1, 2, Chapter 4:Section 2, 3, 4)**	**L1,L2**
Module -3	
BasicConceptsofNumberTheoryandFiniteFields: Groups,RingsandFields,Finitefields oftheformGF(p),PrimeNumbers,Fermat'sandEuler'stheorem,discretelogarithm. **(Text 1: Chapter 3 and Chapter 7: Section 1, 2, 5)**	**L1,L2**
Module -4	
ASYMMETRICCIPHERS: PrinciplesofPublic-KeyCryptosystems,TheRSAalgorithm, Diffie - Hellman Key Exchange, Elliptic Curve Arithmetic, Elliptic Curve Cryptography **(Text 1: Chapter 8, Chapter 9: Section 1, 3,4)**	**L1,L2,L3**
Module -5	
Pseudo-Random-SequenceGeneratorsandStreamCiphers: Linear Congruential Generators, Linear Feedback Shift Registers, Design and analysis of stream ciphers, Stream ciphers using LFSRs, A5, Hughes XPD/KPD, Nanoteq, Rambutan, Additive generators, Gifford, Algorithm M,PKZIP**(Text 2: Chapter16**)	**L1,L2, L3**

Course Outcomes: After studying this course, students will be able to:

- Explain basic cryptographic algorithms to encrypt and decrypt thedata.
- Usesymmetricandasymmetriccryptographyalgorithmstoencryptanddecrypttheinformation.
- Apply concepts of modern algebra in cryptographyalgorithms.
- Apply pseudo random sequence in stream cipheralgorithms.

Question paper pattern:

- Examinationwillbeconductedfor100markswithquestionpapercontaining10fullquestions,eachof20 marks.
- Each full question can have a maximum of 4 subquestions.
- Therewillbe2fullquestionsfromeachmodulecoveringallthetopicsofthemodule.
- Studentswillhavetoanswer5fullquestions,selectingonefullquestionfromeachmodule.
- Thetotalmarkswillbeproportionallyreducedto60 marksasSEEmarksis60.

Text Books:

1. WilliamStallings,"CryptographyandNetworkSecurityPrinciplesandPractice",PearsonEducationInc., 6th Edition, 2014, ISBN:978-93-325-1877-3
2. BruceSchneier,"AppliedCryptographyProtocols,Algorithms,andSourcecodeinC",WileyPublications, 2nd Edition, ISBN:9971-51-348-X.

Reference Books:

1. Cryptography and Network Security, Behrouz A. Forouzan, TMH,2007.
2. Cryptography and Network Security, Atul Kahate, TMH,2003.

B. E. ECE
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
SEMESTER – VII

MACHINE LEARNING WITH PYTHON

Subject Code	**18EC745**	IA Marks	40
Number of Lecture Hours/Week	03	Exam Marks	60
Total Number of Lecture Hours	40	Exam Hours	03

CREDITS –03

Course Learning Objectives: This course will enable students to

- Definemachinelearningandproblemsrelevantto machinelearning.
- Differentiatesupervised,unsupervisedandreinforcementlearning
- Apply neural networks, Bayes classifier and k nearest neighbor, for problems appear in machine learning.
- Perform statistical analysis of machine learningtechniques.

Module – 1	**Teaching Hours**
Introduction: Well posed learning problems, Designing a Learning system,Perspectiveand IssuesinMachineLearning. **Concept Learning:** Concept learning task, Concept learning as search, Find-S algorithm, Version space, Candidate Elimination algorithm, InductiveBias. **PythonlibrariessuitableforMachineLearning:** NumericalAnalysisandDataExplorationwith NumPy Arrays, and Data Visualization withMatplotlib **Text Book1, Sections: 1.1 – 1.3, 2.1-2.5, 2.7**	**10 Hours**
Module – 2	
Decision Tree Learning: Decision tree representation, Appropriate problems for decision tree learning, Basic decision tree learning algorithm, hypothesis space search in decision tree learning, Inductive bias in decision tree learning, Issues in decision tree learning. Example program inPython **Text Book1, Sections: 3.1-3.7**	**10 Hours**
Module – 3	
Artificial Neural Networks: Introduction, Neural Network representation, Appropriateproblems,Perceptrons,Backpropagationalgorithm.ExampleprograminPython **Text book 1, Sections: 4.1 –4.6**	**08 Hours**
Module – 4	
Bayesian Learning: Introduction, Bayes theorem, Bayes theorem and concept learning, ML and LS error hypothesis, ML for predicting probabilities, MDL principle, Naive Bayes classifier,Bayesianbeliefnetworks,EMalgorithm,ExampleprograminPython. **Text book 1, Sections: 6.1 – 6.6, 6.9, 6.11, 6.12**	**10 Hours**
Module – 5	
Evaluating Hypothesis: Motivation, Estimating hypothesis accuracy, Basics of sampling theorem, General approach for deriving confidence intervals, Difference in error of two hypothesis, Comparing learning algorithms. **Instance Based Learning:** Introduction, k-nearest neighbor learning, locally weighted regression, radial basis function, cased-based reasoning, **ReinforcementLearning:** Introduction,LearningTask,QLearningExampleprograminPython. **Text book 1, Sections: 5.1-5.6, 8.1-8.5, 13.1-13.3**	**12 Hours**

Course Outcomes: After studying this course, students will be able to

- Identify the problems in machinelearning.
- Select supervised, unsupervised or reinforcement learning for problemsolving.
- Applytheoryofprobabilityandstatistics in machinelearning
- Applyconceptlearning,ANN,Bayesclassifier,knearestneighbor
- Performstatisticalanalysisofmachinelearningtechniques.

Question paper pattern:

- The question paper will have tenquestions.
- There will be 2 questions from eachmodule.
- Eachquestionwillhavequestionscoveringallthetopicsunderamodule.
- Thestudentswillhavetoanswer5fullquestions,selectingonefullquestionfromeachmodule.

Text Books:

1. Tom M. Mitchell, Machine Learning**,** India Edition 2013, McGraw Hill Education.

Reference Books:

1. Trevor Hastie, Robert Tibshirani, Jerome Friedman, h The Elements of Statistical Learning, 2nd edition, springer series instatistics.
2. EthemAlpaydın,Introductiontomachinelearning,secondedition,MITpress.
3. https://www.analyticsvidhya.com/blog/2015/04/comprehensive-guide-data-exploration-sas-using-python-numpy-scipy-matplotlib-pandas/
4. https://www.oreilly.com/library/view/python-for-data/9781491957653/ch01.html

B. E. ECE
ChoiceBasedCreditSystem(CBCS)andOutcomeBasedEducation(OBE) SEMESTER – VII

COMPUTER NETWORKS LAB

Course Code	**18ECL76**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**02Hr Tutorial(Instructions) + 02 Hours Laboratory**	**SEE Marks**	**60**
RBT Levels	**L1, L2, L3**	**Exam Hours**	**03**

CREDITS – 02

Course Learning Objectives: This course will enable students to:

- ChoosesuitabletoolstomodelanetworkandunderstandtheprotocolsatvariousOSIreferencelevels.
- Design a suitable network and simulate using a Network simulatortool.
- Simulate the networking concepts and protocols using C/C++programming.
- Model the networks for different configurations and analyze theresults.

Laboratory Experiments

PART-A: Simulation experiments using NS2/ NS3/ OPNET/ NCTUNS/ NetSim/QualNet or any other equivalent tool

1. Implementapointtopointnetworkwithfournodesandduplexlinksbetweenthem.Analyzethenetwork performance by setting the queue size and varying thebandwidth.
2. Implementafournodepointtopointnetworkwithlinksn0-n2,n1-n2andn2-n3.ApplyTCPagentbetween n0-n3 and UDP between n1-n3. Apply relevant applications over TCP and UDP agents changing the parameter and determine the number of packets sent byTCP/UDP.
3. ImplementEthernetLANusingn(6-10)nodes.Comparethethroughputbychangingtheerrorrateanddata rate.
4. ImplementEthernetLANusingnnodesandassignmultipletraffictothenodesandobtaincongestion window for different sources/destinations.
5. ImplementESSwithtransmissionnodesin WirelessLANandobtaintheperformanceparameters.
6. Implementation of Link state routingalgorithm.

PART-B: Implement the following in C/C++

1. Write a program for a HLDC frame to perform the following.
i) Bitstuffing
ii) Characterstuffing.
2. Write a program for distance vector algorithm to find suitable path for transmission.
3. Implement Dijkstra's algorithm to compute the shortest routingpath.
4. Forthegivendata,useCRC-CCITTpolynomialtoobtainCRCcode.Verifytheprogramforthecases
   a. Withouterror
   b. Witherror
5. Implementation of Stop and Wait Protocol and Sliding WindowProtocol
6. Write a program for congestion control using leaky bucketalgorithm.

Course outcomes: On the completion of this laboratory course, the students will be able to:

- Illustrate the operations of network protocols and algorithms using C programming.
- Utilize the network simulator for learning and practice of networking algorithms.
- Build the network with different configurations to measure the performance parameters.
- Develop the data link and routing protocols using C programming.
- Develop wired and wireless LAN protocol using network simulator

Conduct of Practical Examination:

- All laboratory experiments are to be included for practicalexamination.
- Forexaminationonequestionfromsoftwareandonequestionfromhardwareoronlyonehardware experiments based on the complexity to beset.
- Students are allowed to pick one experiment from thelot.
- Strictlyfollowtheinstructionsasprintedonthecoverpageofanswerscriptforbreakupofmarks.
- ChangeofexperimentisallowedonlyonceandMarksallottedtotheprocedureparttobemadezero.

B. E. ECE
ChoiceBasedCreditSystem(CBCS)andOutcomeBasedEducation(OBE)
SEMESTER –VII

VLSI LAB

Course Code	**18ECL77**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**02Hr Tutorial(Instructions) + 02 Hours Laboratory**	**SEE Marks**	**60**
RBT Levels	**L1, L2, L3**	**Exam Hours**	**03**

CREDITS – 02

Course Learning Objectives: This course will enable students to:

- Design, model, simulate and verify CMOS digitalcircuits
- Design layouts and perform physical verification of CMOS digitalcircuits
- PerformASICdesignflowandunderstandtheprocessofsynthesis,synthesisconstraintsandevaluating the synthesis reports to obtain optimum gate levelnetlist
- Perform RTL-GDSII flow and understand the stages in ASICdesign

Experimentscanbeconductedusinganyofthefollowingorequivalentdesigntools: Cadence/Synopsis/Mentor Graphics/Microwind

Laboratory Experiments
Part – A
Analog Design

UseanyVLSIdesigntoolstocarryouttheexperiments,uselibraryfilesandtechnologyfilesbelow180 nm.

1. a) Capture the schematic of CMOS inverter with load capacitance of 0.1pF and set the widths of inverter withWn=Wp,Wn=2Wp,Wn=Wp/2andlengthatselectedtechnology.Carryoutthefollowing:
   a. Set the input signal to a pulse with rise time, fall time of 1ns and pulse width of 10ns and time period of20nsandplottheinputvoltageandoutputvoltageofdesignedinverter?
   b. FromthesimulationresultscomputetpHL,tpLHandtdforallthreegeometricalsettingsofwidth?
   c. Tabulatetheresultsofdelayandfindthebestgeometryforminimumdelayfor CMOSinverter?

1. b)Draw layout of inverter with Wp/Wn = 40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

2. a) Capture the schematic of 2-input CMOS NAND gate having similar delay as that of CMOS inverter computed in experiment 1. Verify the functionality of NAND gate and also find out the delay td for all four possiblecombinationsofinputvectors.Tabletheresults.Increasethedrivestrengthto2Xand4Xandtabulate theresults.

2.b)Draw layout of NAND withWp/Wn = 40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

3.a) Capture schematic of Common Source Amplifier with PMOS Current Mirror Load and find its transient response and AC response? Measures the Unity Gain Bandwidth (UGB), amplification factor by varying transistor geometries, study the impact of variation in width to UGB.

1. b) Draw layout of common source amplifier, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record theobservations.

4. a)Capture schematic of two-stage operational amplifier and measure thefollowing:
   a. UGB
   b. dBbandwidth
   c. Gain margin and phase margin with and without couplingcapacitance
   d. Usetheop-ampintheinvertingandnon-invertingconfigurationandverifyitsfunctionality
   e. StudytheUGB,3dBbandwidth,gainandpowerrequirementinop-ampbyvaryingthestagewise

transistor geometries and record the observations.

4.b)Drawlayoutoftwo-stageoperationalamplifierwithminimumtransistorwidthsetto300(in180/90/45nm technology), choose appropriate transistor geometries as per the results obtained in 4.a. Use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare theresults with pre-layout simulations. Record the observations.

Part - B

Digital Design

Carry out the experiments using semicustom design flow or ASIC design flow, use technology library 180/90/45nm and below

Note: The experiments can also be carried out using FPGA design flow, it is required to set appropriate constraints in FPGA advanced synthesis options

1. Writeverilogcodefor4-bitup/downasynchronousresetcounterandcarryoutthefollowing:
   a. Verify the functionality using testbench
   b. Synthesize the design by setting area and timing constraint. Obtain the gate level netlist, find the critical path and maximum frequency of operation. Record the area requirement in terms of number ofcellsrequiredandpropertiesofeachcellintermsofdrivingstrength,powerandarearequirement.
   c. Performtheabovefor32-bitup/downcounterand identifythecriticalpath,delayofcriticalpath,and maximumfrequencyofoperation,totalnumberofcellsrequiredandtotalarea.

2. Writeverilogcodefor4-bitadderandverifyitsfunctionalityusingtestbench.Synthesizethedesignby settingproperconstraintsandobtainthenetlist.Fromthereportgeneratedidentifycriticalpath,maximum delay,totalnumberofcells,powerrequirementandtotalarearequired.Changetheconstraintsandobtain optimum synthesis results.

3. Write verilog code for UART and carry out thefollowing:
   a. Perform functional verification using testbench
   b. Synthesize the design targeting suitable library and by setting area and timing constraints
   c. Forvariousconstrainsset,tabulatethearea,poweranddelayforthesynthesizednetlist
   d. Identifythecriticalpathandsettheconstraintstoobtainoptimumgatelevelnetlistwith suitableconstraints

4. Writeverilogcodefor32-bitALUsupportingfourlogicalandfourarithmeticoperations, use case statement and if statement for ALU behavioralmodeling.
   a. Perform functional verification using testbench
   b. Synthesizethedesigntargetingsuitablelibrarybysettingareaandtimingconstraints
   c. Forvariousconstrainsset,tabulatethearea,poweranddelayforthesynthesizednetlist
   d. Identifythecriticalpathandsettheconstraintstoobtainoptimumgatelevelnetlistwith suitableconstraints

   Compare the synthesis results of ALU modeled using IF and CASE statements.

5. Write verilog code for Latch and Flip-flop, Synthesize the design and compare the synthesis report (D, SR, JK).

6. Forthesynthesizednetlistcarryoutthefollowingforanytwoaboveexperiments:
   a. Floor planning (automatic), identify the placement ofpads
   b. Placement and Routing, record the parameters such as no. of layers used for routing, flip method for placement of standard cells, placement of standard cells, routes of power and ground, and routing of standardcells
   c. Physical verification and record the LVS and DRCreports
   d. Perform Back annotation and verify the functionality of thedesign
   e. GenerateGDSIIandrecord thenumberofmasksanditscolorcomposition

Course Outcomes: On the completion of this laboratory course, the students will be able to:

- Model basic digital circuits, simulate and synthesize using EDA Tool.
- Make use of logic gates to realize shift registers and adders to meet desired parameters.
- Construct and generate layout structure for basic CMOS circuits like inverter, common source amplifier and differential amplifier.
- Experiment with the basic amplifiers to design higher level circuits like operational amplifiers and analog/digital converters to meet desired parameters.
- Inspect concepts of DC Analysis, AC Analysis and Transient Analysis in analog circuits.

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B. E. ECE
ChoiceBasedCreditSystem(CBCS)andOutcomeBasedEducation(OBE) SEMESTER – VII

COMMUNICATION THEORY

Course Code	**18EC751**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**3**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (8Hours/Module)**	**Exam Hours**	**03**

CREDITS – 03

Course Learning Objectives: This course will enable students to:
- Describe essential elements of an electroniccommunications.
- Understand Amplitude, Frequency & Phase modulations, and Amplitudedemodulation.
- Explain the basics of sampling andquantization.
- Understand the various digital modulationschemes.
- The concepts of wirelesscommunication.

Module -1	**RBT Level**
Introduction to Electronic Communications: Historical perspective, Electromagnetic frequency spectrum, signal and its representation, Elements of electronic communications system, primary communication resources, signal transmission concepts, Analog and digital transmission, Modulation, Concept of frequency translation, Signal radiation and propagation **(Text 1: 1.1 to1.10)**	**L1, L2**
Module -2	
Noise: Classification and source of noise **(TEXT1:3.1)** **Amplitude Modulation Techniques:** Types of analog modulation, Principle of amplitude modulation, AM power distribution, Limitations of AM, **(TEXT 1: 4.1,4.2, 4.4, 4.6)** **Angle Modulation Techniques:** Principles of Angle modulation, Theory of FM-basic Concepts, Theory of phase modulation **(TEXT1: 5.1,5.2, 5.5)** **Analog Transmission and Reception:** AM Radio transmitters, AM Radio Receivers **(TEXT1:6.1,6.2)**	**L1, L2**
Module -3	
Sampling Theorem and pulse Modulation Techniques: Digital Versus analog Transmissions, Sampling Theorem, Classification of pulse modulation techniques, PAM, PWM, PPM, PCM, Quantization of signals **(TEXT 1: 7.1 to 7.8)**	**L1, L2**
Module -4	
Digital Modulation Techniques: Types of digital Modulation, ASK,FSK,PSK,QPSK **(TEXT 1: 9.1 to 9.5)** **Source and Channel Coding:** Objective of source coding, source coding technique, Shannon's source coding theorem, need of channel coding, Channel coding theorem, error control and coding **(TEXT 1: 11.1 to 11.3, 11.8, 11.9,11.12)**	**L1,L2**
Module -5	
Evolution of wireless communication systems: Brief History of wireless communications, Advantages of wireless communication, disadvantages of wireless communications, wireless network generations, Comparison of wireless systems, Evolution of next-generation networks, Applications of wireless communication**(TEXT 2: 1.1 to 1.7)** **Principles of Cellular Communications:** Cellular terminology, Cell structure and Cluster, Frequencyreuseconcept,Clustersizeandsystemcapacity,Methodoflocatingcochannelcells, Frequecy reuse distance**(TEXT 2: 4.1 to4.7)**	**L1, L2**

CourseOutcomes: Attheendofthecourse,studentswillbeable:

- Describeoperationofcommunicationsystems.
- Understand the techniques of Amplitude and Anglemodulation.
- Understand the concept of sampling andquantization.
- Understand the concepts of different digital modulationtechniques.
- Describe the principles of wireless communicationssystem.

Question paper pattern:

- Examinationwillbeconductedfor100markswithquestionpapercontaining10fullquestions,eachof20 marks.
- Each full question can have a maximum of 4 subquestions.
- Therewillbe2fullquestionsfromeachmodulecoveringallthetopicsofthemodule.
- Studentswillhavetoanswer5fullquestions,selectingonefullquestionfromeachmodule.
- Thetotalmarkswillbeproportionallyreduced to60marksasSEEmarksis60.

Text Book:

1. AnalogandDigitalCommunicationsbyTLSingal,McGrawHillEducation(India)PrivateLimited.
2. WirelessCommunicationsbyTLSingal,McGrawHillEducation(India)PrivateLimited.

Reference Books:

1. ModernDigitalandAnalogCommunicationSystemsB.P.Lathi,OxfordUniversityPress.,4thed,2010,
2. CommunicationSystems:AnalogandDigital,R.P.SinghandS.Sapre:TMH2ndedition,2007
3. IntroductiontoWirelessTelecommunicationssystemsandNetworksbyGrayJMullett,Cengage learning.

B. E. EC/TC
ChoiceBasedCreditSystem(CBCS)andOutcomeBasedEducation(OBE) SEMESTER – VII

NEURAL NETWORKS

Course Code	**18EC752**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**Exam Marks**	**60**
Total Number of Lecture Hours	**40 (08 Hours per Module)**	**Exam Hours**	**03**

CREDITS – 03

Course Learning Objectives: This course will enable students to:

- Understand the basics of ANN and comparison with Humanbrain.
- AcquireknowledgeonGeneralizationandfunctionapproximationofvariousANNarchitectures.
- Understand reinforcement learning using neuralnetworks
- Acquire knowledge of unsupervised learning using neuralnetworks.

Module -1	**RBT Level**
Introduction: Biological Neuron – Artificial Neural Model -Types of activation functions – **Architecture**: Feedforward and Feedback, Convex Sets, Convex Hull and Linear Separability, Non-Linear Separable Problem. XOR Problem, Multilayer Networks. **Learning:** Learning Algorithms, Error correction and Gradient Descent Rules, Learning objective of TLNs, Perceptron Learning Algorithm, Perceptron Convergence Theorem.	**L1,L2**
Module -2	
Supervised Learning: Perceptron learning and Non Separable sets, α-Least Mean Square Learning, MSE Error surface, Steepest Descent Search, μ-LMS approximate to gradient descent, Application of LMS to Noise Cancelling, Multi-layered Network Architecture, Backpropagation Learning Algorithm, Practical consideration of BP algorithm.	**L1,L2,L3**
Module -3	
Support Vector Machines and Radial Basis Function: Learning from Examples, Statistical Learning Theory, Support Vector Machines, SVM application to Image Classification, Radial Basis Function Regularization theory, Generalized RBF Networks, Learning in RBFNs, RBF application to face recognition.	
Module -4	
Attractor Neural Networks: Associative Learning Attractor Associative Memory, Linear Associativememory,HopfieldNetwork,applicationofHopfieldNetwork,BrainStateinaBox neural Network, Simulated Annealing, Boltzmann Machine, Bidirectional Associative Memory.	**L1,L2,L3**
Module -5	
Self-organizationFeatureMap: MaximalEigenvectorFiltering,ExtractingPrincipal Components, Generalized Learning Laws, Vector Quantization,Self -organization Feature Maps, Application of SOM, Growing Neural Gas.	**L1,L2,L3**

Course Outcomes: At the end of the course, students should be able to:

- Understandtheroleofneuralnetworksinengineering,artificialintelligence,andcognitivemodelling.
- Understandtheconceptsandtechniquesofneuralnetworksthroughthestudyofthemostimportant neural networkmodels.
- Evaluate whether neural networks are appropriate to a particularapplication.
- Applyneuralnetworkstoparticularapplication,andtoknowwhatstepstotaketoimproveperformance.

Question paper pattern:

- Examinationwillbeconductedfor100markswithquestionpapercontaining10fullquestions,eachof20 marks.
- Each full question can have a maximum of 4 subquestions.
- Therewillbe2fullquestionsfromeachmodulecoveringallthetopicsofthemodule.
- Studentswillhavetoanswer5fullquestions,selectingonefullquestionfromeachmodule.
- Thetotalmarkswillbeproportionallyreduced to60 marksasSEEmarksis60.

Text Book:

NeuralNetworksAClassroomApproach–SatishKumar,McGrawHillEducation(India)Pvt.Ltd, SecondEdition.

Reference Books:

1. **IntroductiontoArtificialNeuralSystems**-J.M.Zurada,JaicoPublications1994.
2. **Artificial Neural Networks**- B. Yegnanarayana, PHI, New Delhi1998.