K. S. INSTITUTE OF TECHNOLOGY

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Faculty Name	Dr.Anita P
Designation	Asst. prof.
Educational Qualification	Ph.D
Experience in Years	13.5
Areas of Interest	VLSI and Embedded system
E-mail	anitap@ksit.edu.in

Educational Details

Examination/ Degree	College / University	Year of Passing
Ph.D.	The oxford college of engineering/VTU	2024
M.Tech	CMRIT,VTU	2013
BE	GVIT,BU	2002

Publications

Journal Publications:

1 .Anita P, Manju Devi, “An Efficient Range Enhanced Packet Classification Module to Improve the Computational Performance on FPGA”, International Journal of Electrical and Computer Engineering (IJECE) Vol.12, no.6, December 2022, ISSN: 2088-8708, DOI: 10.1159/ijece.v12i6.pp5840-5847. (Scopus indexed).

2 .Anita P, Manju Devi, "High performance modified bit-vector based packet classification module on low-cost FPGA," International Journal of Electrical and Computer Engineering(IJECE), 12, No. 6, Dec 2022 ,3855-3863 (Q2 Scopus indexed),Vol. 12, No. 6, December 2022, pp. 5840~5847,ISSN: 2088-8708, DOI: 10.11591/ijece.v12i6.pp5840-5847.

3.Anita P, Manju Devi, "Design of a Low Latency and High Throughput Packet Classification Module on FPGA Platform", International Journal of Innovative Technology and Exploring Engineering (IJITEE), ISSN:2278-3075, Volume- 9 Issue- 6, pp.1468-1474. April 2020 (Scopus indexed).

4. "AIRCRAFT DETECTION USING PASSIVE MULTISTATIC RADAR", International Journal of Advanced Research in Science and engineering (IJARSE) ISSN: 2319:8354 Vol.4, Issue No.12, Dec 2015.

5. "Hardware Implementation of Wave Pipelining Backtracking Switch for Optimizing NCOs," International Journal of Advanced Information Science and Technology (IJAIST) ISSN: 2319-682, Vol.12, No.12, April 2013.

6. "Design of Binary CSD multiplier using ASIC front end", International conference on communication, VLSI & Signal processing", Feb. 20- 22, 2013.

7."Flexible TCP/IP Packet Generation framework", Nation Conference May 2013, New Horizon, B' lore

8. "Implementation of Binary canonical signed digit multiplier using application specific Integration Circuits" International Journal of engineering research and application (IJERA) –March 5th Issue-2013.

Conference Papers :- -

Patents Filed :

Awards

5 Years survive award at CMRIT.

Professional Membership

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Contact Details

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