K.S. INSTITUTE OF TECHNOLOGY, BANGALORE – 560109

DEPARTMENT OF COMPUTER AND COMMUNICATION ENGINEERING

Report on Workshop

"VERILOG HDL"

Date of Conduction: 18th and 19th January 2024

Venue: KSIT Online lab, 4thFloor

Time:10:00AM –4:00 PM

Duration: 14 Hours.

Expert Details – with photo

Name: Padmanaban K.

Designation: Software Enabling &Optimization Engineer,

Organization: Intel Technologies India PVT. LTD.,

Place: Bangalore

Brief Profile about the Expert:

Padmanaban has been working as the Software Enabling and Optimization Engineer in the Customer Experience Group at Intel PSG for the past 3 years. He is the academic ambassador for the Intel India FPGA University Program. Padmanaban has a postgraduate degree in Applied Electronics from Anna University, Chennai, and a Bachelor in EEE from GCT, Coimbatore. He has 16+ years of experience in digital design for both FPGA and ASIC. Prior to joining Intel, he worked as a Chief Faculty in Sandeepani School of VLSI design (Training division of CoreEL Technologies, Bangalore) for 8 years and as an Assistant Professor and Project Coordinator at Ramaiah University of Applied Sciences (RUAS) Bangalore for 5 years

Sl. NO	Contents
1	Aim of the workshop
2	Abstract of the workshop
3	Introduction to basics of Digital System
4	Design in details Description Design of Describe System Hardware Description Languages Logic Simulations Things which can & can’t be translated. The Role of HDL Design Methodologies &Types of HDL Verilog HDL vs. VHDL
5	Verilog HDL & its history Verilog Data Types in Details Operators, Procedural Constructs, Event-Control &Loop Statements
6	Verilog Module Description &Test Benches Verilog Modelling in Details
7	Main points to remember & some tips for Verilog HDL Coding
8	Conclusion Question &Answer (QNA)Session Practical example on computer
9	Experience from the workshop session.

Objectives / Key Highlights: To make the students

- To understand about the Verilog HDL.
- To Analyze, Synthesize, and Simulate Lab Programs.
- To execute the Lab programs using ModelSim software**.**

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Participant details - No. of Participants: 50
Students (internal):45
Faculty: 5

1. Aim of the workshop

1). To make the students to understand about the Verilog Hardware Description Language (which is included as a part of Digital Design and Computer Organization (1BCS302) in the III semester).
2). To provide an interactive session with the industry people.
3). To create an aware of the importance of co-curricular activities in
engineering domain

2. Abstract of the workshop session

Initially session dealt with the basic concepts of digital system design. Then the concepts of Verilog HDL were related with C Programming & complete details on Verilog HDL with examples were discussed.

3. Introduction to Basics of Digital System

The construction of different systems, the designs which are nothing but the specification of requirement, difference between small devices (like flip-flops) & large circuit (like microprocessors).
The hardware description languages are used to design the large & advanced circuit such as micro-controllers & microprocessors etc.The usage of the variable, constants & logics etc. in Verilog HDL are similar to C Language.

4. Design in Details

Design is the specification of requirement as discussed earlier. Design can be of different levels such as:

1. SwitchLevel
2. Register Transfer Level
3. Instruction Set Architecture Level etc.

For the design to check whether it is working or notA. Simulation& B.Synthesis isdone.

Description:

Ifthe simulation is successfullthenthe design is working & then it canbe synthesized wherethenetlistiscreated.Thisnetlistgivesoutthelistofthe components to be used.

Design of Describe System:

Thevery1st stepafterthedescriptionofsystemis howtodesignthe describe system. It includes:

- DesignSpecification
- DesignSimulation
- DesignSynthesis

Hardware Description Language:

A **hardware description language (HDL)** is a specialized computer language used to describe the structure and behavior of electronic circuits, and most commonly, digital logic circuits.
A hardware description language looks like a programming languagesuchasC; it is a textual description consisting of expressions, statements and control structures. One important difference between most programming languages and HDLs is that HDLs explicitly include the notion of time.
The functionalworkingofHDLis parallel way.

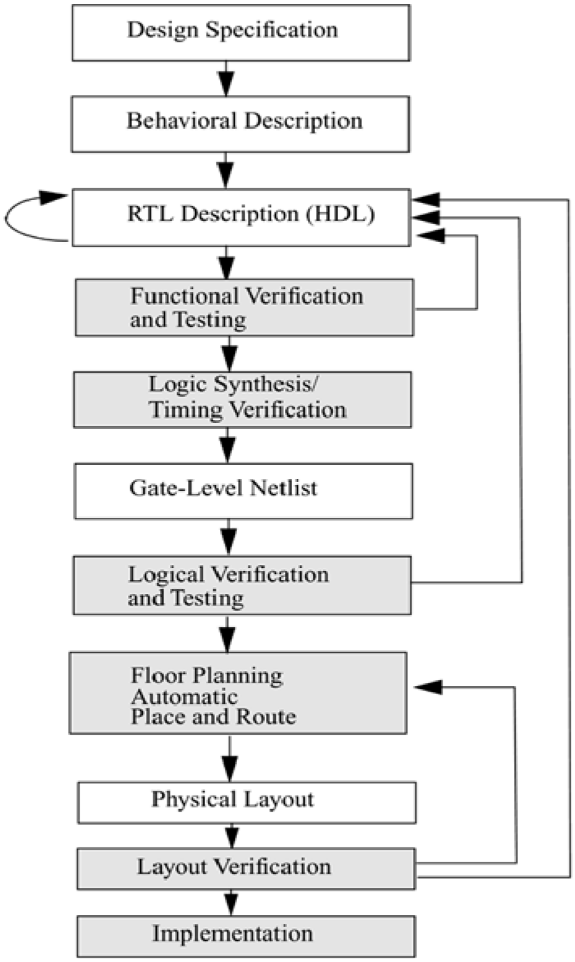

Design Specification
Behavioral Description
RTL Description (HDL)
Functional Verification and Testing
Logic Synthesis/ Timing Verification
Gate-Level Netlist
Logical Verification and Testing
Floor Planning Automatic Place and Route
Physical Layout
Layout Verification
Implementation

Fig: design of the describe system

Logic Simulation:

It gives the output for the design made for specification. We can modify any gate by verifying the truth table & waveforms. It includes the fabrication of the devices & also we can make our own devices.

Things which can &can't be translated:

Translation isconversionofinputtooutput.Thethingswhichcanbetranslated are:

- Structural Definitions
- BehavioralBlocks
- UserDefinedFunction(Blocks)etc.

The things which can't be translated are:

- InitialBlocks
- Delays
- Varietyofotherobscure languagefeaturesetc.

TheRoleofHDL :

Thelanguage helps to describe any digital circuit in the form of structural, behavioraland gate level and it is foundtobeanexcellentprogramming language for FPGAs and CPLDs.

Thusithasfollowingroles:

- Behavioral
- Structural
- Physical

DesignMethodologies&TypesofHDL:

Therearetwotypesofdesignmethods:

TopDown

Down Top

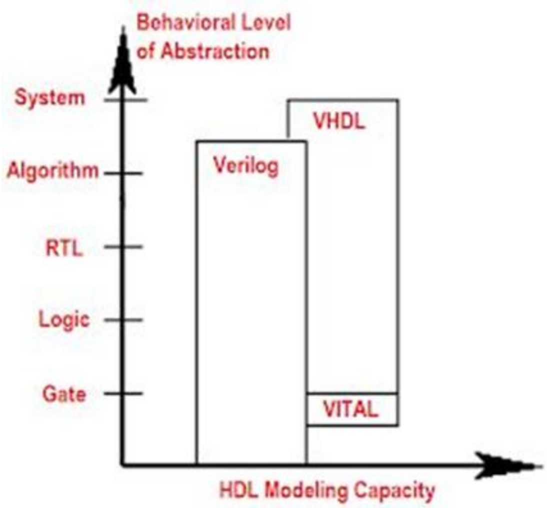
Thesearemainlybasedon Hierarchical Rank.
HerearemainlytwotypesofHardware Description Languageswhichare standardized by IEEE, those are as follows:

- ➢ VHDL/VHSIC HDL (Very High Speed Integrated Circuits HardwareDescriptionLanguage), is discovered by US Department of Defense
- ➢ VerilogHDL,discoveredbyOpenVerilogInternational.

VerilogHDLvs.VHDL:

WhytolearnVerilogHDLinsteadofVHDL?

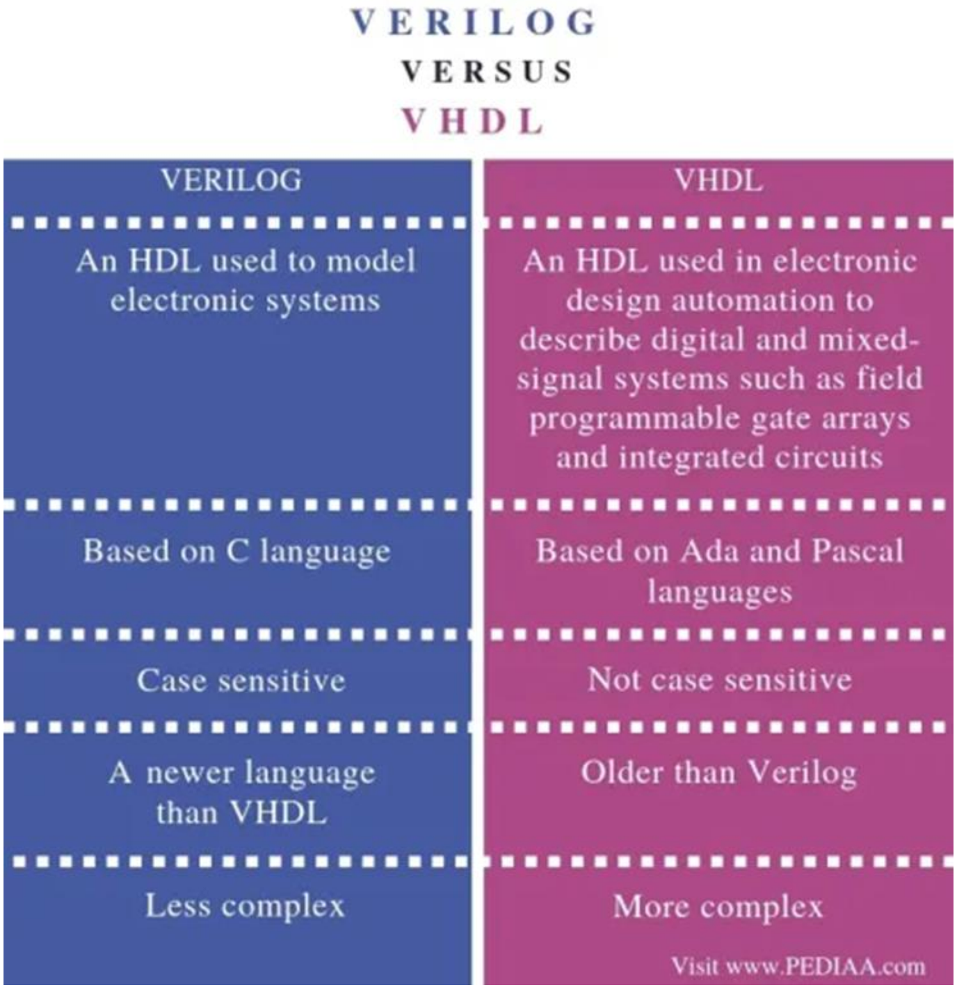
- VerilogHDLgivesbetterlowendthanVHDL
- It ismoremodellinglanguage.



VHDL hasseparateinput&outputblockswhereinVerilogHDLhasbothinput & output in the same block.

5. Verilog HDL and Its History

History: Verilog HDL was invented by Phil Moor by and Prabhu Goelaround 1984. It served as a proprietary hardware modeling language owned byGateway Design Automation Inc. At that time, the language was not standardized. It modified itself inalmost allthe revisions that came out between 1984 to 1990.



VERILOG
VERSUS
VHDL

VERILOG	VHDL
An HDL used to model electronic systems	An HDL used in electronic design automation to describe digital and mixed-signal systems such as field programmable gate arrays and integrated circuits
Based on C language	Based on Ada and Pascal languages
Case sensitive	Not case sensitive
A newer language than VHDL	Older than Verilog
Less complex	More complex

Visit www.PEDIAA.com

Fig:: Difference between VHDL and Verilog

6. Verilog Module

Definition: Verilog, standardized as **IEEE 1364**, is ahardware description language (HDL) used to model electronic systems.

Use: It is most commonly used in the design and verification of digital circuits at the register-transfer levelofabstraction. It is also used in the verification ofanalog circuits and mixed-signal circuits, as well as in the design of genetic circuits.

Features: Itiscasesensitive& parallel programcompilingfunction.

Verilog Data Types in Details:

Thereareprimarilytwodatatypes:

- Nets
- Registers(IntegerReal&Timer)

Nets: The internalconnections ofa block diagramexcept for input & output are called nets.Netsare represented as wires.

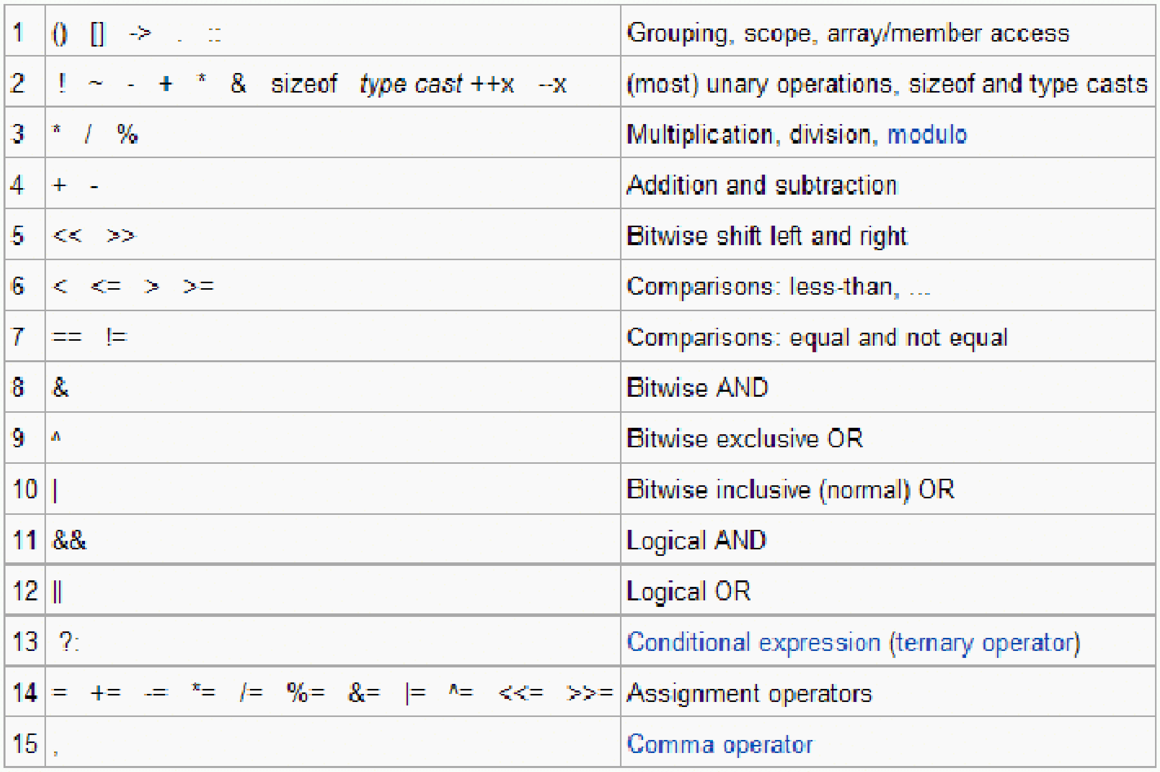
Registers: Thefunctionofregistersisstoringdata&showingtheresult until next input is selected,such as integers,real & timer etc.

- **Integers:**Integershavedefaultwidthof32bits.Thesearedeclaredbykeyword ‘integer’.
- **Real:**Realnumber,constants&variablesare declared usingkeyword‘real’.

- **Time:** Aspecialtime register data type is used in Verilog to store simulation time.
- **Arrays:**Theseareallowedforreg,integer&time,notallowedforreal variables.
- **Strings:**Canbestored inreg.Eachcharacterinstringrequires8bitsof storage.

Operators,ProceduralConstructs&LoopStatements:

Operators: Theoperatorsaresameas'C'Programmingoperatorsasshown in figure
Below



1	() [] -> . ::	Grouping, scope, array/member access
2	! ~ - + * & sizeof *type cast* ++x --x	(most) unary operations, sizeof and type casts
3	* / %	Multiplication, division, modulo
4	+ -	Addition and subtraction
5	<< >>	Bitwise shift left and right
6	< <= > >=	Comparisons: less-than, ...
7	== !=	Comparisons: equal and not equal
8	&	Bitwise AND
9	^	Bitwise exclusive OR
10	|	Bitwise inclusive (normal) OR
11	&&	Logical AND
12	||	Logical OR
13	?:	Conditional expression (ternary operator)
14	= += -= *= /= %= &= |= ^= <<= >>=	Assignment operators
15	,	Comma operator

.

- **ProceduralConstructs:**
  - InitialStatement(Evaluateonlyonce)
  - Always Statement (Evaluate inaloopmanner)
- **LoopStatement:**
  - Repeat
  - While
  - For

Description & Test Benches:

A module represents a design unit that implements specific behavioural characteristics and will get converted into a digital circuit during synthesis.
Any combination of inputs can be given to the module, and it will provide a corresponding output.It allows the same ***module*** to be reused to form more significant modules that implement more complex hardware.

Hardware Schematic

Instead of building up smaller blocks to form bigger design blocks, the reverse process can also be done.

Consider the breakdown of a simple GPU engine into smaller components such that each can be represented as a module that implements a specific feature.

```
  module <name> ([port_list]);
            // Contents of the module
endmodule
        // A module can have an empty portlist
module name;
      // Contents of the module
endmodule
```

ii.TestBenches: Implementsinglemodelformanyinput withoutwritingmanually.

Verilog Modelling in Details:

Thereare mainlythreetypesofmodellinginVerilogHDLasfollows:

- Gaatelevelmodelling(LogicGates)
- DataFlowmodelling(AssignBooleanexpressions)
- Behavioralmodelling(Result)

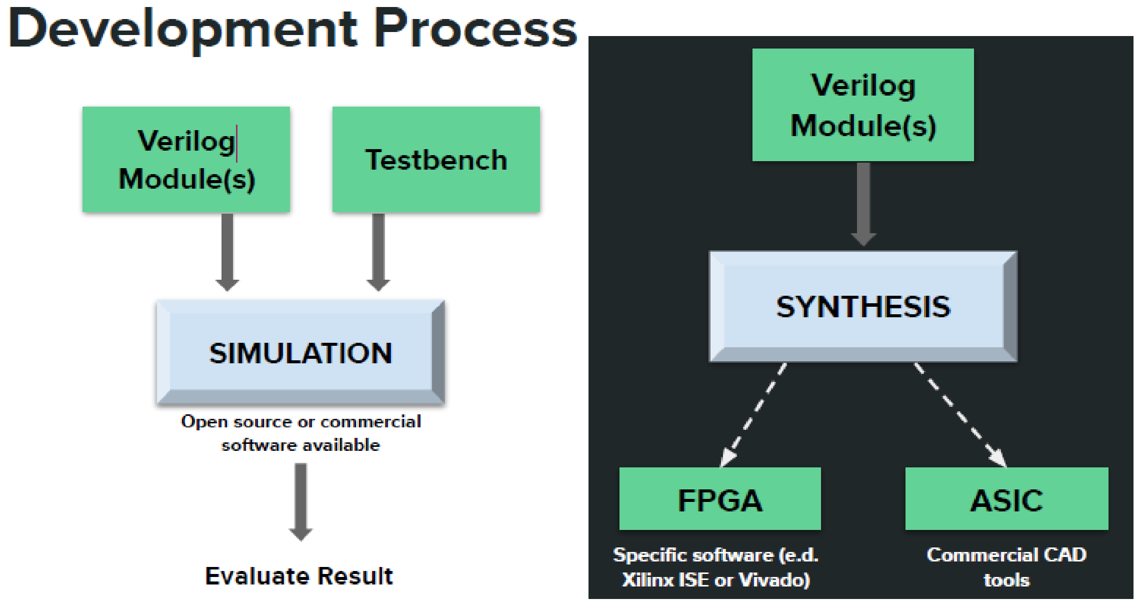


Fig: Development and Synthesis Process

7. Main points to remember & some tips for Verilog HDL Coding

Mainpointstoremember:

Verilogisconcurrent.

Thinkwhilewritingtheprogram-planforrequirement.

Blocking&UnblockingCode.

Tips:Don’ts	Does
Don’tWrite‘C’code Thinkhardware,notalgorithm Verilog is inherently parallel, Compilersdon’tmapalgorithmtocircuit.	Dodescribehardwarecircuits Firstdrawadataflowdiagram Then start coding

8. Conclusion:

The sessionwas concluded withsome questions and answers & practicalcoding example in computer. I asked different questions toPadmanaban K. sir about Verilog coding’s and sir cleared all the doubt with satisfactory answers.

Question & Answer (QNA)Session:

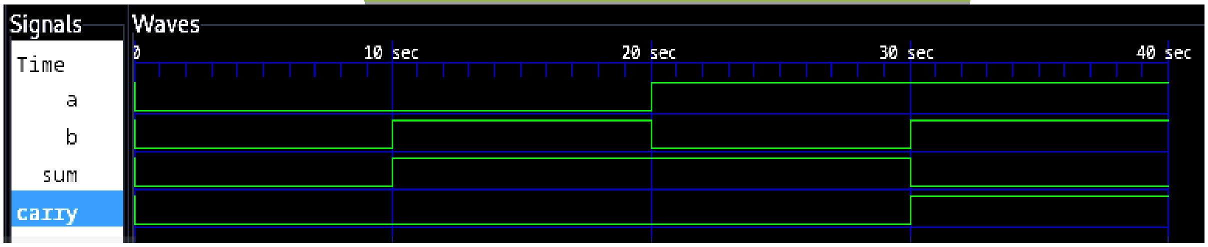
i). Whatisdone forreducingverylargecircuittransistor?
Answer: The channel length is reduced.
ii). Question:Isthe‘Always’statementhassameworkedasanyotherloop?
Answer: Yes,itissimilar to ‘for’,‘while’& ‘do while’loop.But themain thing to be keep in mind is conditions.
iii).Question:WhichstyleofVerilogcodingisbeingusedthemost?
Answer: There is nothing a particular style like structural,dataflow or behavioralstyle is used,foranyspecificationthe mixedofanyofthesethreeare used.

Practical example on computer:

Ahalfadder modulecodingwas showninthreedifferentcodingstyles practically and its output.The codesare as follows:

```
moudleHalf_adder(a,b,sum,carry)

//DataFlowStyle
input a,b;
outputsum, carry;

assign sum =a^b;
assigncarry =a&b;

//StructuralStyle
xor(sum,a,b);
and(carry,a,b);

//Behavioral Style
if a='0';
b='0';
then sum=0;
carry=0;
else
sum=1;
carry=0;
```

Input/Output:



Photos:

GPS Map Camera
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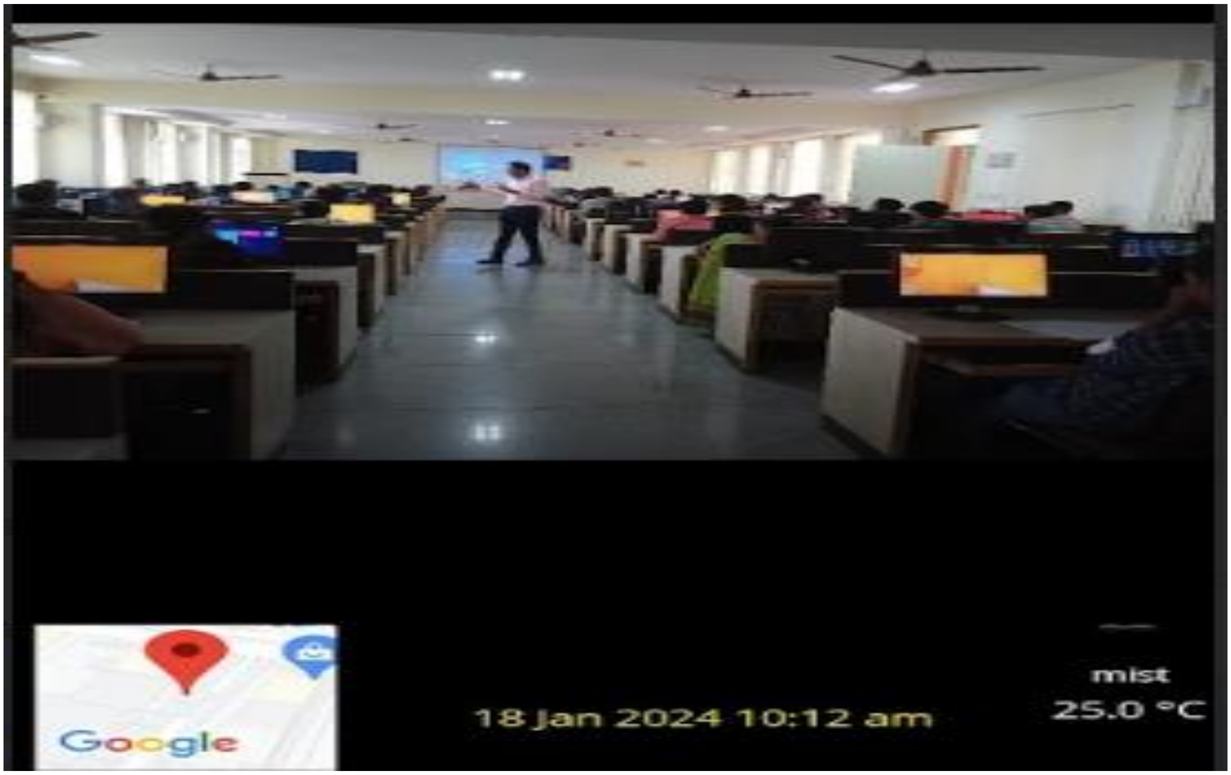
Final day photo with Principal, Padmanabhan K,HOD and students



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Students Executing the Verilog code in the workshop

1. N bit adder (parameter)
2. 2:1/4:1/8:1- using both if else and case (6)
3. D-Latch
4. DFF- Posedge and Negedge
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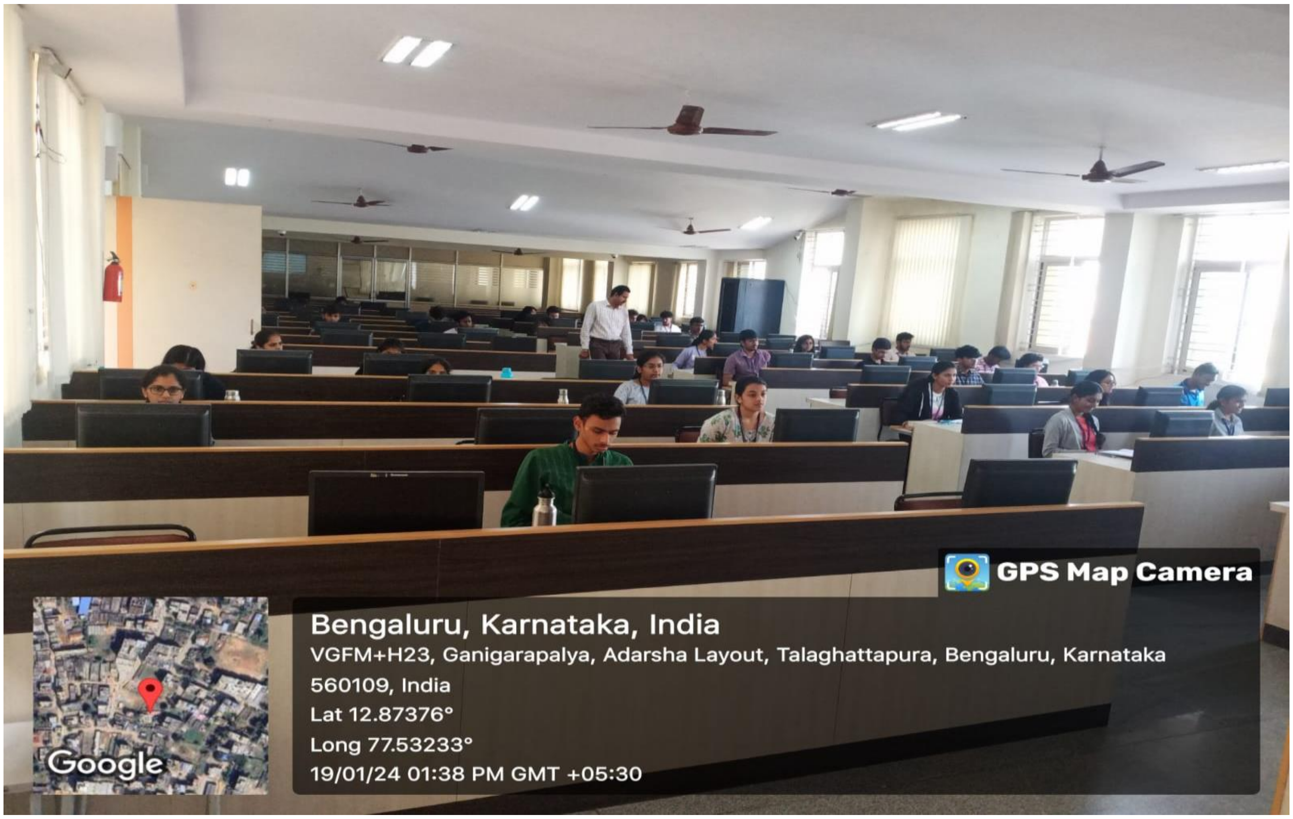
Students listening in the workshop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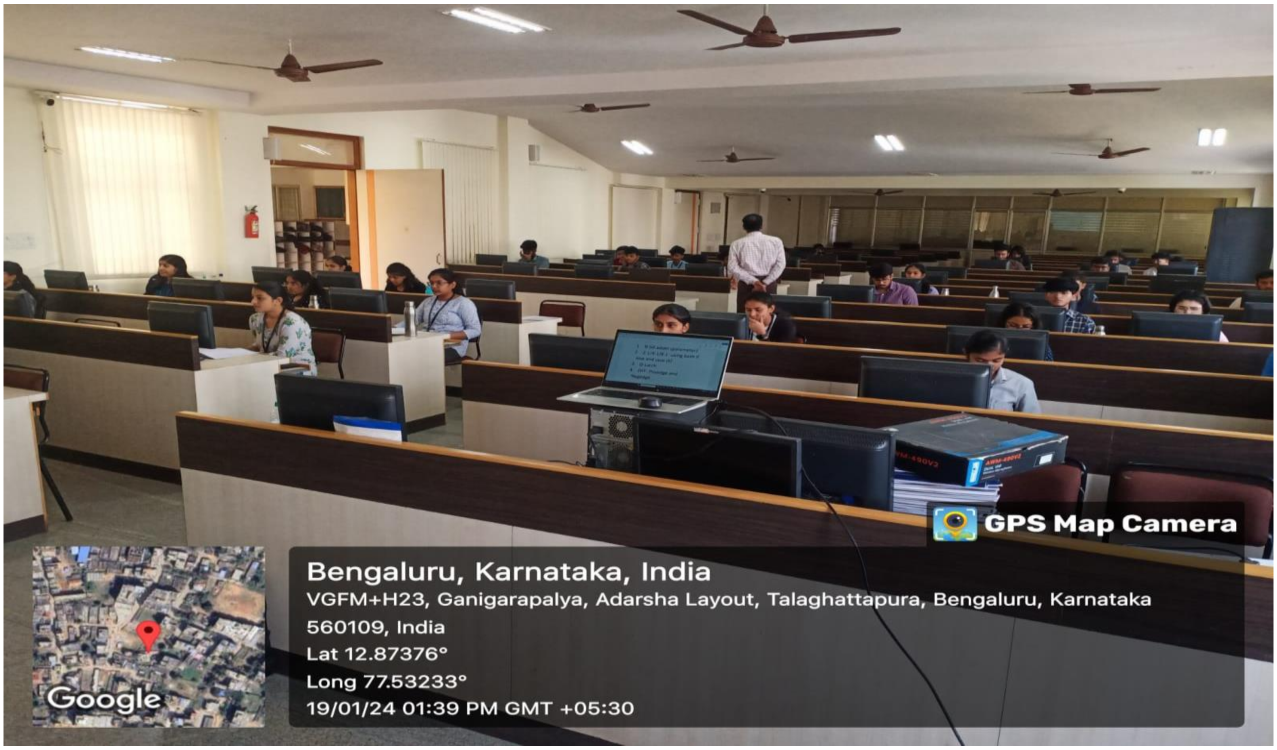
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9. Experience from the Work shop.

It was an informative, interesting and a successful workshop session. As a student of Computer& Communication Engineering, we understood the importance of Verilog HDL within Two days. I Express my thanks to Mr.Padmanaban K.who spent his valuable time for us. We also thank you to our respected Principal sir,HOD madam and our Managementfor arranging such an informative program. Finally, I would like to thank full to my colleagues and our students to make this work shop very successful.

Outcomes / Benefits:

- Studentsunderstoodaboutthe Verilog-HDL.
- Studentsgainedtheknowledgeonthe Verilog-HDL coding and Simulation.

Attachments:

1. CommunicationwithResourceperson
2. ResourcepersonProfile
3. EvaluationandFeedback

CO/PO&PSOmapping-CCE

CO/ PO& PSO	PO1	P02	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
Event (Work shop)	-	-	3	-	3	2	-	-	2	3	-	3	2	2

PSO1: To understand and apply the concepts to design and develop solutions in computer and communication Engineering.

PSO2: To use the inculcated experiential learning for research and develop inventivesolutions for societal benefit while ensuring security with moral values and ethics.

Shashikala H.C. Event Coordinator	**Dr.ChandaV. Reddy** Head-CCE	**Dr.DilipKumarK.** Principal, KSIT