IEEE CCEM 2019

September 19-20, 2019

The Oterra, 43, Electronics City,
Hosur Road, Bangalore

Call for Student Project Showcase

From 19th September 2019 5PM onwards

The Student Project Showcase offers an opportunity for under-graduate and graduate students to do more constructive academic projects to analyse how cloud computing can be leveraged to assuage problems of emerging markets. Reviewed and accepted proposals will have a dedicated space for presentation and demos.

The CCEM Conference has showcased innovative technologies implemented by students in their projects in previous years as well and these sessions have been very interactive with the conference audience. Student Project proposals should typically include an overview of the technology innovations being leveraged, top use cases for the innovations, comparison to competing technologies and alternatives, architecture, design and implementation challenges as well as a link to a three minute or less uploaded Youtube video demo.

Please follow the paper/proposal template mandatorily as given in the website. The top six submissions will have an opportunity to present the Student Project Proof-of-Concept (PoC) before the conference participants. The best PoC presentation will win the "8th IEEE CCEM 2019 Student Project Showcase PoC Competition Award". **Please Note: Student Project Proposal authors are strictly restricted to students only.**

Submission Link:
https://easychair.org/conferences/?conf=ieeeccem2019

Visit http://2019.ieeeccem.org for more details

Are you that engineering student who has just graduated - having done a wonderful project that demonstrates an useful innovation in the world of DL/ML/IoT/AI using cloud?

Are you project students experimenting with new innovation ideas using cloud services or modifying such & have come across insights whose results you would like to share?

For the 30 best submissions selected after due review FROM ALL SUBMISSIONS, the first author will be registered free for half day on 19th Sept. Other co-authors must a half-day registration for 19th Sept to participate. This half-day registration includes state of art 2-hr lightning Tutorials by delivered by senior technologists from Microsoft &VMware as well being eligibile for best Student Project PoC Showcase Award and dinner. For submission details please check the website http://2019.ieeeccem.org It just takes few hours to write your project showcase proposal & make a youtube video.

On Scholarships sponsorer recommendation, Student Project Showcase submissions deadline has been extended from 9th to 15th Sept 2019

Some of the Topics of Interest in this Conference include Technologies & applications with Cloud /Big Data/ AI/ Deep Learning/ IoT, both for & from Emerging Markets.

Additionally, the areas of path-breaking innovative application interest include:

Affordable Healthcare: Eco-systems, Devices Management, e-Health Data, e-Health Networks
Swachha Bharat: Clean & Green Environments & Spaces,
Leveraging IndiaStack & digital payment solutions
Smart cities - Intelligent management of Resources
Affordable Security and Privacy of data
Intelligent Automation of IT Systems & Processes

APPLY NOW!

Discover the **Newest Trends,**
Breakthroughs and **Innovations**
in **Cloud Technologies** at
8th IEEE CCEM 2019

Securing Distributed SDN Controller Network from Induced DoS Attacks

Shravanya G
Department of Computer Science and Engineering
PES University
Bengaluru, India
shravanya.g17@gmail.com

Swati N H
Department of Computer Science and Engineering
PES University
Bengaluru, India
swatinagaraj2@gmail.com

Ram P Rustagi
Department of Computer Science and Engineering
KS Institute of Technology
Bengaluru, India
rprustagi@ksit.edu.in

Oshin Sharma
Department of Computer Science and Engineering
PES University
Bengaluru, India
oshinsharma40@gmail.com

***Abstract*—With the escalation in security breaches on organizations and institutions that store, maintain and work with critical data, there is a need for a security-enhancing and risk-mitigating solution that works on the fly and is feasible to implement. Software Defined Networks is a networking paradigm that makes the network agile by disaggregating hardware and software. SDN helps enhance security with the help of micro-segmentation. The controller maintains a central view of the network, and its ability to monitor and store network information helps optimize routing. The centralization nature of the controller makes it vulnerable to DoS attacks which can be catastrophic for network functioning. The objective of this paper is to secure the distributed SDN controller architecture against DoS attacks. The proposed architecture is robust, scalable, and uses Big Data techniques to process streams of network traffic in real-time and Machine Learning to detect and mitigate DoS attacks.**

***Index Terms*—Software Defined Networks, DoS Attack, RyuController, Zodiac FX, Kafka, Storm**

I. Introduction

Software Defined Networking (SDN) is a state-of-the-art networking architecture that got traction on account of its features such as dynamism, manageability, cost-effectiveness and adaptability. These features make SDNs suitable to be used with big data, cloud computing and other similar networking services which demand high-bandwidth, dynamic architecture and improved performance which the traditional network paradigm fails to provide[1]. The SDN architecture is a three-layered architecture[2] consisting of data or infrastructure layer, control layer and application layer in the order as shown in Fig. 1 below. The data plane layer (or infrastructure layer) consists of the hardware components of the network and carries the responsibility of packet forwarding functionality. The control layer consists of the software components of the network which are responsible for installing flow tables and controlling the logic behind forwarding functionality. The entity which implements the control plane is called SDN Controller. The application layer refers to various network applications and services that govern forwarding functionality. The two layers - data plane and control plane layer represent the disaggregation between the hardware and software components of the network. The control layer provides a central view of the entire network topology and thus becomes the hub of central intelligence[3].

The implementation of network flows based on SDN paradigm is different from the network flows of the legacy networks owing to the three-layered architecture. In the SDN paradigm, the data plane processes all the traffic received from the hosts connected to it (SDN network infrastructure layer) and forwards as per flow tables. In the legacy network, there is no separation of control plane and data plane.

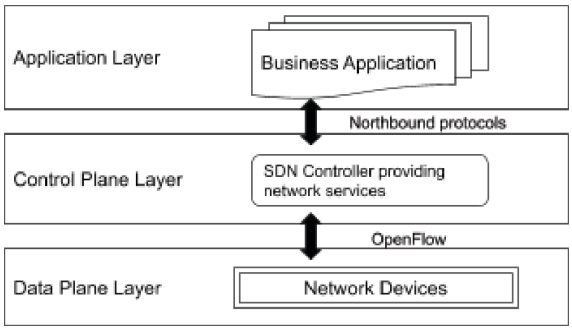


Fig. 1. Three-layered architecture of SDN

The data plane relies on the flow tables information received from the SDN controller (control plane layer) to carry out the packet forwarding functionality[4]. In case a flow table entry is not available for new traffic, the data plane sends OpenFlow[5] request messages to the SDN controller for new flows entries so that it can process this traffic and forward accordingly. The controller responds with applicable flow entries that are installed in the forwarding flow tables in the data plane enabling it to complete its forwarding functionality as shown in Fig. 2.

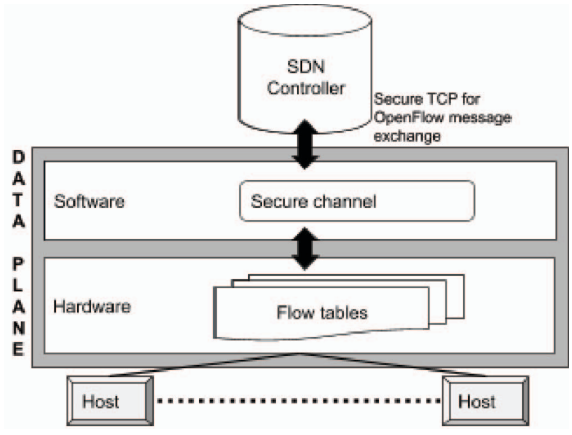


Fig. 2. OpenFlow communication between SDN switch and controller

978-1-7281-6334-5/19/$31.00 ©2019 IEEE
DOI 10.1109/CCEM48484.2019.000-4

2019 International Conference on Smart Systems and Inventive Technology (ICSSIT 2019)

Tirunelveli, India
27 – 29 November 2019

Pages 1-651

IEEE Catalog Number: CFP19P17-POD
ISBN: 978-1-7281-2120-8

Second International Conference on Smart Systems and Inventive Technology (ICSSIT 2019)
IEEE Xplore Part Number: CFP19P17-ART; ISBN:978-1-7281-2119-2

Plant leaf segmentation through connected pixel approach

Dr. Dayanand R B
Professor, Department of Computer Science,
KSIT, Bengaluru
Email-dayanandarb@ksit.edu.in

Daneshwari A Noola
Assistant Professor, Department of Information Science, BLDEACET, Vijayapura
Email- daneshwari_a@rediffmail.com

Abstract-Agricultural plays a significant role in human survival and it has become much more essential due to population increase and food demand, and hence the crop yield has to be produced according to the demand. However, one of the reason that quality and quantity of the crop gets compromised is the disease and in past various methodology has been proposed, however they lack on the various model metrics or the segmentation is achieved for the particular leaf, . In this paper, we have proposed a methodology named as SCPA (Segmentation through Connected Pixel Approach). The main objective of this paper is to achieve high accuracy segmentation. SCPA is the two step approach first we find the ROI(Region of Interest) of the particular leaf and in the second approach we find the instance based ROI i.e. for the whole plant, here both the step are performed simultaneously through incorporating one another. Moreover, SCPA is optimized iterative-based method and it is achieved through the approach of connected pixel approach. Connected pixels are the one where the edge of one pixel is connected to the other. When performed on the LSC dataset we achieve the accuracy of 95.10 %. This methodology is compared with the various state of art model and existing system by considering the model metric such as SBD, the results shows that SCPA model performs better than the other exiting method also the pictorial comparison of segmented leaf are shown and it shows our model identify it well when compared to others.

Keywords: ROI (Region of Interest), segmentation, Plant Leaf segmentation

1 INTRODUCTION

In recent survey, it is found that economy of India highly depends on the agricultural productivity. Moreover, this is one the reason where detecting the disease has become one of the eminent task in recent days [1]. Negligence in this area causes the serious issue to the plant and these results in compromise in quantity, quality and productivity of crop [2]. Moreover, the traditional method for detecting the plant disease is through the eye observation by experts, to do that one need big team of experts that can monitor the plant all the time. Traditional method does not work in efficient manner, as it is costly, hence

The automatic detection of disease is required as it is efficient, accurate and cheaper.

In plants, there are several visible disease such as colored spots scorch, bacterial and fungal disease. This type of disease are visible and can be detected through the image processing technique.

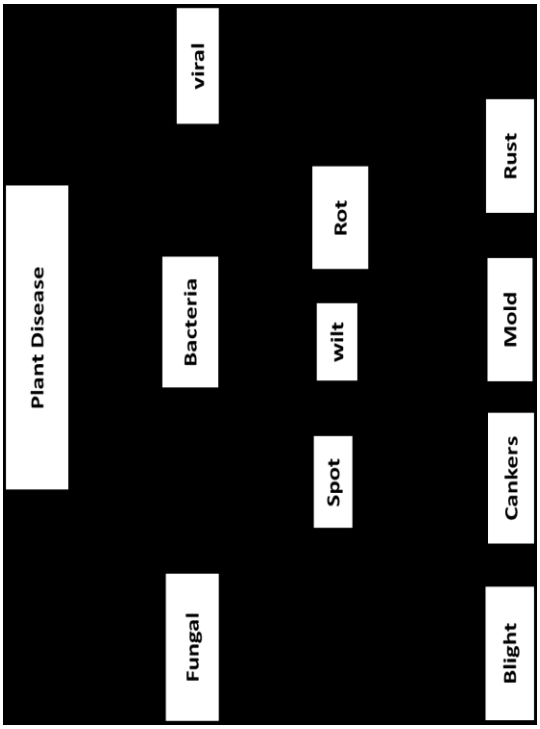


Figure 1 Types of plant Disease

The above diagram shows the different types of plant leaf disease, the figure shows the classification of various leaf disease. Moreover the plant disease caused due to the biotic agents.Plant disease are classified into three types based on the reason of the disease i.e. fungal, Bacteria and Viral. Moreover fungal is sub classified into various disease such as Blight, cankers, Mold and Rust whereas Bacteria is sub classified into disease such as spot wilt and root. All these disease causes the reduction in quality of the crops.

In order to detect the plant leaf disease, image-processing technique is one of the popular technique, which detects the disease accurately. Generally any image process follow 5 steps process to classify any

Authorized licensed use limited to: UNIVERSITY OF BIRMINGHAM. Downloaded on June 15,2020 at 06:38:00 UTC from IEEE Xplore. Restrictions apply.

Second International Conference on Smart Systems and Inventive Technology (ICSSIT 2019)
IEEE Xplore Part Number: CFP19P17-ART; ISBN:978-1-7281-2119-2

Optimization of Hadoop MapReduce Model in cloud Computing Environment

Vaishali Sontakke
Research Scholar VTU,
Bengaluru.
Email- vaishalisntakke@rediffmail.com

Dr. Dayanand R B
Professor, Department of Computer Science,
KSIT, Bengaluru.
Email-dayanandarb@ksit.edu.in

Abstract-In recent years data analysis has become one of the trending topic among the researchers. Moreover, Information is the new baseline of all organization, as to grow the faster and bigger. Relevant information provides the flexibility to know the like and dislike of customer and to get the relevant information requires the analysis of huge information that is stored in various format. Hadoop constitutes of two basic model i.e. Hadoop Distributed File system (HDFS) and MapReduce, Hadoop is used for processing the huge amount of data whereas MapReduce is used for data processing. Hadoop MapReduce is one of the best platform for processing the huge data in efficient manner such as processing of web logs data. In this paper, we have proposed optimized HPMR (Hadoop MapReduce) model, which maximizes the memory utilization for the task and balances the performance between the I/O system and CPUs. HPMR contains the three phase i.e. Hadoop, Map and Reduce just like any other Hadoop model, however HPMR optimizes all three phase i.e. map, shuffle and reduce. Moreover, to optimize the memory model HPMR opts for dynamic terminology and input/output optimization is done through the dual operation. Moreover, in order to evaluate the performance of our model we have performed the Word-Count application on the Wikipedia data of size 128 Mb, 256 Mb, 512 Mb, 1 GB and 2 GB. The comparative analysis shows that our model optimizes nearly 30% better than the existing one.

Keyword: Optimized HPMR (Hadoop MapReduce) model, Hadoop MapReduce, HDFS (Hadoop Distributed File System).

1 INTRODUCTION

Cloud computing is one of the promising technology in the recent era that gives the demand service for analyzing, storing and processing of the data [1]. Moreover, in order to achieve the absolute scalability and achieve the better performance one needs the flexible distributed on the cloud environment. Big data helps in gathering the data and aggregating the huge amount of data to understand the data for the better decision making [2][3][4].

In recent the most popular approach for such big data analytics is used which is named as MapReduce [5] along with its implementation known as Hadoop. Hadoop allows the analyzing of data without any complexity and huge installations through the Virtual Machine and storage, which is hosted by the cloud. Hence, one can easily create the MapReduce virtually and cluster to analyze the data. Moreover, he MapReduce is used for parallel processing the data on various applications [6] [7]. MapReduce is a simple programming model which is used for processing the large dataset through two function i.e. Map () and Reduce ().

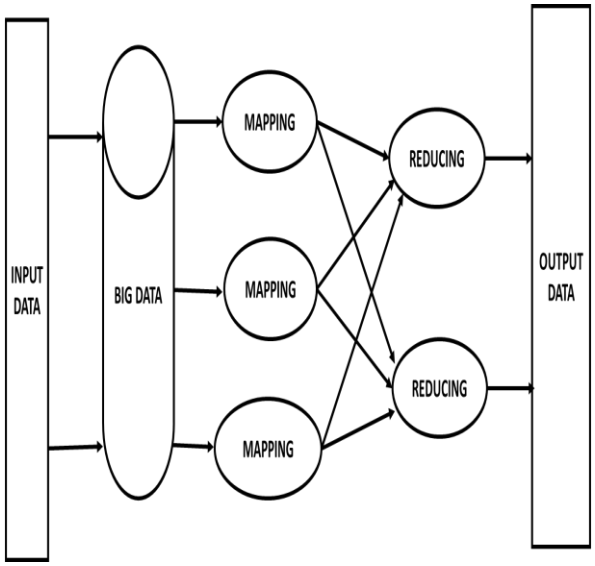


Figure 1 Hadoop MapReduce architecture

Figure 1 shows the Hadoop MapReduce architecture; here the Map function uses the pairs of (key, value) to generate the intermediate pairs (key, value). This pair act as the input to Reduce function for producing the final output. MapReduce constitutes two steps: MAP and Reduce. Map functions:

Step1: It reads the input as a problem and parts into the sub -problems.

Step2: Distributes the sub-problems to the worker node.

Step3: The worker node sends the outcome t the master node.

2019 International Conference on Communication and Electronics Systems (ICCES 2019)

Coimbatore, India
17 – 19 July 2019

Pages 1-700

IEEE Catalog Number: CFP19AWO-POD
ISBN: 978-1-7281-1262-6

Proceedings of the Fourth International Conference on Communication and Electronics Systems (ICCES 2019)
IEEE Conference Record # 45898; IEEE Xplore ISBN: 978-1-7281-1261-9

An effective security protocol for GDS (group Data sharing) in Healthcare Cloud Environment

Uma Hombal
Department of CSE
Research Scholar, KSIT Bengaluru
uhombal@gmail.com

Dr. R. B. Dayananda
Department of CSE
KSIT, Bengaluru
rbdayanandakit@gmail.com

Abstract: **The data-sharing in cloud computing will enable many users to share the data. This helps in accessing the information easily and to share the data efficiently. The healthcare data will have to be shared amongst different healthcare centers and the medical practitioners. This involves security issues while sharing the healthcare data within a group. We provide the group model for sharing of data that is based on block based design where the group members will perform the key agreement to get the common group key that helps to shares the data securely. The fault tolerant property is provided by this design which can detect the malicious attackers during the group data sharing. The proposed group data-sharing is compared with the existing data sharing models w.r.t. the time cost of computation for group key generation and sharing of data.**

Keywords— Cloud computing, group data sharing, block based design, key agreement.

I. INTRODUCTION

The Personal health has been brought the great concern in modern residents. The population development and aging, the influence of health-care dictate and demands require for novel and the advanced solutions. At greater integration scale and lower cost, the availability of the computing re-sources has profited healthcare practices. With the help of development and success of the internet that plays an eminent role in maximizing the quality and access so the process is interrelated to the healthcare, which is determine the ICTs (Information of Communication Technologies) [1]. The E-health is defined as the ICTs application to the healthcare, which has come in normal use. While, these ICTs models can be considering many significance in the domain of healthcare, on top of the specific number of ICTs which is based on the emerged paradigm of health-care. There is a widespread use of electronic health record (EHR) [2]. Cloud computing is one of the popular health-IT infrastructures for facilitating EHR sharing. Healthcare providers and all the insurance companies store the electronic medical records in centralized databases .This includes maintaining health records, monitoring of patients etc.

The E-health can be widely defined as the ICTs application to the healthcare that has come in normal use. The co-operation between specialists in terms of the health experts, who can be working together efficiently, and generated their management in sharing and activities their information about the victim easier and in normal manner, and thus they can give cure to the patients. The systems of health are enable for citizen to have control their own health. However, there are security and privacy issues related to the health-care data. The security and privacy protection of cross-institutional electronic patient records is of major importance. The major concern is security in EHR networked systems and for communicating patient data. Here the physical security, network security, application security, internal systems security, secure data-backup strategy, secure internal policies and procedures, third-party certification are considered.

In this paper, our aim is to confirm the security of information sharing within a group in health care cloud security network. Here multiple data owners can freely share the outsourced data with high security. The entity authentication services are provided. The fault detection and fault tolerance is performed to identify the malicious user. We present the block design based key agreement protocol by extending the structure of the symmetric block design to support multiple participants. It enables multiple data owners to freely share the outsourced data. Here the adaptive symmetric block design is constructed as the group data-sharing model to support group data sharing in cloud computing. Here each group member performs the key agreement to derive a common group key to ensure the security of the outsourced group data. The help of group members can produce the normal group key. The semi-trusted and attackers of cloud server has no access to create the key. Cloud Security Service Third Party Verifier takes responsibility for the cloud storage auditing and key updates.

This paper is organized in such a way in section-II Literature survey, section- III described our proposed method, in section- IV, evaluation and medical outcome that is represented and in section- V conclusion.

NEW HORIZON COLLEGE OF ENGINEERING

Autonomous College Permanently Affiliated to VTU, Approved by AICTE & UGC
Accredited by NAAC with 'A' Grade, Accredited by NBA

The Trust is a Recipient of Prestigious Rajyotsava State Award 2012 Conferred by the Government of Karnataka
Awarded Outstanding Technical Education Institute in Karnataka-2016
Ring Road Bellandur Post Near Marathalli Bangalore -560 103 INDIA

TOP ENGINEERING COLLEGE OF INDIA as per
NATIONAL INSTITUTIONAL RANKING FRAMEWORK, 2018
Ministry of Human Resource Development, Government of India

AICTE SPONSORED

International Conference On

"Innovative Research in Engineering, Management and Sciences"

(ICIREMS - 2019)

19th to 21st December 2019

All reviewed papers will be published in UGC approved journals and selected paperswill be published in Springer, IETE Journal, Institution of Engineers(India), Scopus, Web of Science

New Horizon College of Engineering
Outer Ring Road, Marathahalli,
Bangalore – 560103

www.newhorizonindia.edu

Knowledge Partners

Industry Partners

International Conference on Innovative Research in Engineering, Management and Sciences
International Journal of Scientific Research in Computer Science, Engineering and Information Technology
© 2019 IJSRCSEIT | Volume 4 | Issue 9 | ISSN : 2456-3307

Enhancement of Signature Schemes for Heightening Security in Blockchain

Prof M ShanmugamShoba*[1], Dr. Rekha B Venkatapur[2]
*[1]Senior Assistant Professor, Information Science & Engineering Department, NHCE, Bangalore, India
[2]Professor & Head, CSE, KSIT, Bengaluru, India
reach2shobhamahe@gmail.com/mshanmugams@newhorizonindia.edu[1]

ABSTRACT

Blockchain has become one of the most pioneering technologies, with the rise of Bitcoin, blockchain which is the core technology of Bitcoin has received increasing attention. There are multiple signature scheme based on digital signature schemes that supports making signatures on many different messages generated by many different users, the size of the signature could be shortened by compressing multiple signatures into a single signature. Based on the blockchain architecture and existing Merkle tree based signature schemes, In this paper, an analysis of how to enhance the signature schemes to secure the transactions on blockchain based on extensible post-quantum (PQ) resistant digital signature scheme best suited to blockchain and distributed ledger technologies is proposed.

I. INTRODUCTION

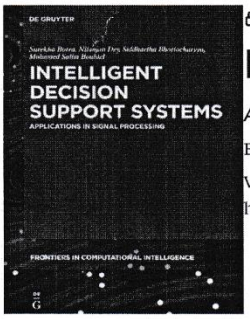
Recent advances in quantum computing and the threat this poses to classical cryptography has increased the interest in PQ research. More specifically, due to Shor's algorithm [1], a quantum computer could easily factor a big integer in polynomial time, thus effectively break RSA. Implementations of Shor's algorithm can also solve discrete logarithms and render today's digital signatures, such as DSA, ECDSA and EdDSA, useless[2].

The race to build quantum computers has already begun and companies like Google, Microsoft, IBM, D-Wave and Intel are at the forefront. That being said, we have yet to build a computer with the thousands of stable qubits that are required to make classical public key cryptography obsolete. However, there is significant progress in the field and some optimistic predictions estimate that a large quantum computer capable of breaking asymmetric cryptography might be available in the next10to20years[3],[4].

The security impact of breaking public key cryptography would be tremendous, as almost everything from HTTPS, VPN and PKI in general, is basing their authentication, key exchange and digital signatures on the security of RSA or Elliptic Curve Cryptography (ECC). Blockchains would be hit equally hard resulting in broken keys that hold coins/assets, and would perhaps be one of the most affected sectors because there is economic incentive for hackers to get access to blockchain accounts anonymously.

To address the concern of compromised keys, PQ cryptog- raphy is dealing with the design and evaluation of systems that will survive the quantum

DE GRUYTER



Requires Authentication | Published by **De Gruyter** | 2019

Intelligent Decision Support Systems

Applications in Signal Processing

Edited by: Surekha Borra, Nilanjan Dey, Siddhartha Bhattacharyya and Mohamed Salim Bouhlel

Volume 4 in the series De Gruyter Frontiers in Computational Intelligence
https://doi.org/10.1515/9783110621105

Citations 7

OVERVIEW CONTENTS

About this book

Intelligent prediction and decision support systems are based on signal processing, computer vision (CV), machine learning (ML), software engineering (SE), knowledge based systems (KBS), data mining, artificial intelligence (AI) and include several systems developed from the study of expert systems (ES), genetic algorithms (GA), artificial neural networks (ANN) and fuzzy-

eBook
Published: October 21, 2019
ISBN: 9783110621105

Hardcover
Published: October 21, 2019
ISBN: 9783110618686

Downloaded on 8.4.2024 from https://www.degruyter.com/document/doi/10.1515/9783110621105/html

SPRINGER LINK

Log in

Menu Search Cart

Home > Inventive Computation Technologies > Conference paper

Secrecy Capacity of Symmetric Keys Generated by Quantising Channel Metrics Over a Fading Channel

| Conference paper | First Online: 03 November 2019

| pp 404–413 | Cite this conference paper

Inventive Computation Technologies

(ICICIT 2019)

L. Srividya & P. N. Sudha

Part of the book series: Lecture Notes in Networks and Systems ((LNNS,volume 98))

Included in the following conference series:
International Conference on Inventive Computation Technologies

853 Accesses

Abstract

Copyright information

© 2020 Springer Nature Switzerland AG

About this paper

Cite this paper

Srividya, L., Sudha, P.N. (2020). Secrecy Capacity of Symmetric Keys Generated by Quantising Channel Metrics Over a Fading Channel. In: Smys, S., Bestak, R., Rocha, Á. (eds) Inventive Computation Technologies. ICICIT 2019. Lecture Notes in Networks and Systems, vol 98. Springer, Cham. https://doi.org/10.1007/978-3-030-33846-6_45

.RIS .ENW .BIB

DOI
https://doi.org/10.1007/978-3-030-33846-6_45

Published
03 November 2019

Publisher Name
Springer, Cham

Print ISBN
978-3-030-33845-9

Online ISBN
978-3-030-33846-6

eBook Packages
Intelligent Technologies and Robotics
Intelligent Technologies and Robotics (R0)

Publish with us

Policies and ethics

Recruit researchers Join for free Login

See all ›
14 References

Download citation Share Request full-text

Secrecy Capacity of Symmetric Keys Generated by Quantising Channel Metrics Over a Fading Channel

Chapter · January 2020 *with* 12 Reads
DOI: 10.1007/978-3-030-33846-6_45
In book: Inventive Computation Technologies, pp.404-413
Cite this publication

L. Srividya

Sudha P N
2.28 · K S institute of Technology, Bangalore,India

Abstract

Physical layer security has become the cornerstone of the wireless communication system. Key generation by channel estimation enables legitimate users to generate keys in a decentralised manner than sharing secret information in open wireless mediums. In this paper we propose secrecy evaluation of symmetric keys which are, generated by channel metrics estimated over the Rayleigh fading channel, encrypted and transmitted over a fading channel in the presence of an eavesdropper. The results are obtained in terms of secrecy capacity and outage probability for various key sizes, different position of eavesdroppers from the source. It is seen that as key size increases and distance of eavesdropper increases from the source the secrecy capacity increases. Also the performance of keys derrived from various channel metrics such as complex channel path gains, EVM rms and complex phase difference are discussed in this paper.

Do you want to **read the rest** of this chapter?

Request full-text

Citations (0) References (14)

CERTIFICATE OF PARTICIPATION

This is to certify that

Dr.P.N.Sudha

has presented the paper entitled

Secrecy Capacity of Symmetric Keys Generated by Quantising Channel Metrics Over a Fading Channel

in the 4th International Conference on Inventive Computation Technologies (ICICT - 2019), organized by RVS Technical Campus during August 29 - 30, 2019 at Coimbatore, India.

Session Chair

Conference Chair
Dr. S. Smys

Director
Dr. V. Robinson

SPRINGER LINK

Log in

Menu | Search

Cart

Intelligent System Design pp 827–835

Secure Anti-piracy System

Junaid Khan, Akshatha Shenoy, K. M. Bhavana, Megha S. Savalgi & Surekha Borra

Conference paper | First Online: 11 August 2020

764 Accesses | **1** Citations

Part of the book series: Advances in Intelligent Systems and Computing ((AISC,volume 1171))

Abstract

About this paper

Cite this paper

Khan, J., Shenoy, A., Bhavana, K.M., Savalgi, M.S., Borra, S. (2021). Secure Anti-piracy System. In: Satapathy, S., Bhateja, V., Janakiramaiah, B., Chen, YW. (eds) Intelligent System Design. Advances in Intelligent Systems and Computing, vol 1171. Springer, Singapore. https://doi.org/10.1007/978-981-15-5400-1_78

.RIS .ENW .BIB

DOI	Published	Publisher Name
https://doi.org/10.1007/978-981-15-5400-1_78	11 August 2020	Springer, Singapore

Print ISBN	Online ISBN	eBook Packages
978-981-15-5399-8	978-981-15-5400-1	Intelligent Technologies and Robotics Intelligent Technologies and Robotics (R0)

Publish with us

Policies and ethics

Springer

Dayananda Sagar University

3rd INTERNATIONAL CONFERENCE ON INTELLIGENT COMPUTING AND COMMUNICATION (ICICC-2019)

7th & 8th JUNE, 2019

Organized by

Department of Computer Science and Engineering,

School of Engineering, Dayananda Sagar University, Bengaluru, India.

CERTIFICATE OF APPRECIATION

This is to certify that Prof./Dr./Mr./Ms. Surekha Bora

of K.S. Institute of Technology participated and presented a paper titled Secured Anti-Piracy Screen.

in ICICC-2019 held at Dayananda Sagar University, Bengaluru, India.

Dr. S. C. Satapathy
General Chair

Dr. M. K. Banga
Organizing Chair

Chief Patrons:

Sri. L. Arun Kumar
Hon. Chairman, ATMECE, Mysuru
Sri. K. Shivashankar
Hon. Secretary, ATMECE, Mysuru
Sri. R. Veeresh
Hon. Treasurer, ATMECE, Mysuru
Sri. Venkatesh
Hon. Trustee, ATMECE, Mysuru

Principal:

Dr. L. Basavaraj
ATMECE, Mysuru

Advisory Committee:

Dr. G. Hemantha Kumar
Vice Chancellor, University of Mysuru
Dr. K. Chidananda Gowda
Former Vice Chancellor, Kuvempu University, Karnataka
Dr. Syed Shakeeb ur Rahman
Executive Council Member, VTU, Belagavi
Dr. Eskindir Anteneh Lt. Colonel
Academic Dean, College of Engineering, Defense university, Ethiopia
Dr. Ruzaire Bin Abdul Rahim
Deputy Vice Chancellor (Research & innovation), Universiti Tun Hussein Onn Malaysia (UTHM), Malaysia
Mohd Helmy Abd Wahab
Editor in Chief at Advances in Computing and Intelligent System Journal, University Tun Hussein Onn Malaysia (UTHM), Malaysia
Dr. Shyam Vasudev Rao
Director, Forus Health, Pvt. Ltd, Bangaluru
Prof. M. N. Hoda
Director, Bharati Vidyapeeth's Institute of Computer Applications and Management (BVICAM), New Delhi
Dr. Ajay Thakare
Governing Council Member, IETE- Delhi, Professor and Head, Sipna College of engineering & Technology, Amaravati(M.S.)
Dr. M K Venkatesh
Principal, RNSIT, Bengaluru
Dr. Himamshu Monga
Dean, Directorate of Technical Education, Himachal Pradesh
Dr. Dinesh Rangappa
Professor, Department of Nano -Technology, VTU, Chikballapur
Dr. Lokanath
Professor, Department of Physics, University of Mysuru
Dr. Mahadev Prasanna
Professor, IIIT Dharwad
Dr. Somashekar Hiremath
Professor, Department of Mechanical Engineering, IIT, Chennai

Organizing Committee:

Dr. Parthasarathy L
Professor and Head of the Dept. of EEE, ATMECE
Dr. Rathnakar G
Professor and Head of the Dept. of ME, ATMECE
Dr. Bhagyashree S R
Professor, Dept. of ECE, ATMECE
Dr. Puttegowda D
Professor, Dept. of CSE, ATMECE
Dr. Akshaya B J
Associate Professor, Dept. of CE, ATMECE
Dr. Suresha K J
Associate Professor, Dept. of CE, ATMECE

Important Dates

Last Date for Paper Submission	5th February 2020
Notification of Acceptance	17th February 2020
Registration	5th March 2020
Conference Dates	8th & 9th April 2020

Registration fee

	Indian (Rs)	Foreign (US $)
Industry	4000	250
Academician	3000	200
Research / Ph.D Scholars	2500	150
Student (PG)	2000	100
Student (UG)	1500	100
Delegates	2500	100

For Paper Submission:
https://easychair.org/conferences/?conf=icrtst2020
And for Other Information Please Visit:
http://icrtst.atme.in/

For Further Details Contact :

Dr. Puttegowda D
Professor, Dept. of CSE
Mob: 9900622014

Dr. Akshaya B J
Associate Professor, Dept. of CE
Mob: 9986870588

OR

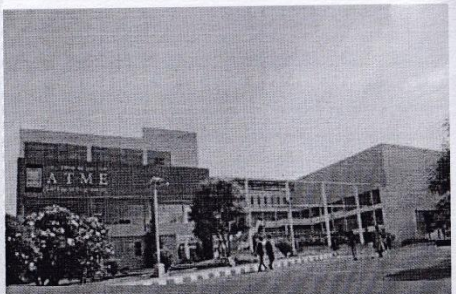
Dr. Srinivasa K	Professor, ME	9945045415
A. C. Pavithra	Assistant Professor, EC	8884699040
Nasreen Fathima	Assistant Professor, CSE	9986617206
Vinod Kumar P	Assistant Professor, EEE	9538006039
Srivathsa H U	Assistant Professor, CV	8867572081

For Accommodation Please Contact:

Dr. Suresha K J
Associate Professor, CV
9845566754

Mr. Rudresh A N
Assistant Professor, CV
9743580290

ATME
College of Engineering



International Conference on

Recent Trends in Science & Technology

ICRTST - 2020

In Association with:

On:
08th & 09th April 2020

Venue:
ATME College of Engineering,
13th KM, Mysore – Kanakapura – Bangalore Road,
Mysore – 570 028.
Phone: +91-821-25 93 335
Fax: +91-821-25 93 328
Web: www.atme.in

A T M E
College of Engineering

INTERNATIONAL CONFERENCE
on Recent Trends in Science & Technology
Date:17th & 18th June 2020
(ICRTST - 2020)

ICRTST 2020

CERTIFICATE

This is to certify that Mr/Mrs/Ms/Dr/Prof ***S Christo Jain***

Visvesvaraya Technological University (VTU)

has presented paper entitled ***Proposal of Wireless Power Transfer System with array of Aerial for short distance applications***

in the "INTERNATIONAL CONFERENCE on Recent Trends in Science & Technology (ICRTST - 2020)" organized by ATME College of Engineering, Mysuru held on 17th and 18th June 2020.

Dr. Parthasarathy L
Organizing Chair, ICRTST-2020
Professor & Head
Dept. of EEE, ATMECE, Mysuru

Dr. Basavaraj L
Principal
ATMECE, Mysuru

e-ISSN: 2395-0056 p-ISSN: 2395-0072

International Research Journal of Engineering and Technology

(An ISO 9001-2008 Certified Journal)

Fast Track Publications

Special Issue ICRTST-2020

International Conference on Recent Trends in Science & Technology-2020 [ICRTST-2020]

Organized by

ATME College of Engineering

Mysuru, Karnataka, India

Date: June 17th & 18th , 2020

01	Proposed OFDM System using Different Modulation Schemes and Varied Cyclic Prefix Length for WIMAX System -Sonika Thakur, Himanshu Monga

Activate Windows

Proposal of Wireless Power Transfer System with array of Aerial for short distance applications

S Christo Jain[1]
Research Scholar
Department of Electronics and Communication
K.S. Institute of Technology
s.christojain@gmail.com

Dr. Manju V C[2]
Professor
Dept of Telecommunication
K S Institute of Technology
manju_tvm@yahoo.com

Abstract

This research work signifies and focuses on reducing the complexity of power transfer. Using this system, we can able to reduce complexity since no wire is required for transmission of electricity. Compared to other systems, using this procedure we can improve the efficiency, decreases the energy crisis and reduces the power loss. Wireless power transmission completely eliminates usage of wires so that we can reduce accidents and electric shocks in the house. In this method we are using Dipole antenna instead of wires for transmission of power.

Keywords: Dipole Aerial, radiating frequency, wireless power transfer

Introduction

In wire power supply pre planning is required to install wires for power supply; As we are using wireless power supply device, we do not require pre planning for installation as this device is flexible. In wide space areas long extension wires are used which make the rooms clumsy and disturbance in walk area may occur, these problems can be avoided in wireless power supply. this device is portable. Using this device, we can avoid the usage of wires. Strong winds can break tree barks or entire trees on transformer causing them to fall on the ground, Severe winds can even break electric lines and poles, bring down a, this problem is not seen in wireless power supply. Transformer explosions can also avoid using Wireless power supply device.

WPT or WET is transmission of electrical energy without using of any physical device among transmitter side to receiver side[2,3].This technology transmitter operated by electrical power from a power source which generates a time varying electromagnet, which transmits power across space to a receiver device, then it supplied to the load through power converter circuit. This technique of wireless power transmission can remove the use of batteries and wires. This method save load from unwanted power and provide safety to the user [5]. One of the difficulties in remaining power system is the victims taking place in the transmission and division of energy to the end users. The supply of the electricity happens through chords to the distribution lines. The major problem faced in wired transmission is power loss due to power converters, controllers and at the nodes.
We are using array of half wave Dipole aerial in the proposed system. A dipole is the simplest and most widely used class of aerial. A dipole aerial commonly consists of two identical conductive elements such as metal wires or rods.

Array of half wave dipole aerial

The half wave dipole antenna is the most popular and simplest version of the dipole aerial or aerial. As the name specifies, the half wave dipole is a half wavelength long. As this antenna has reasonable length radius of the dipole does not affect the input impedance.

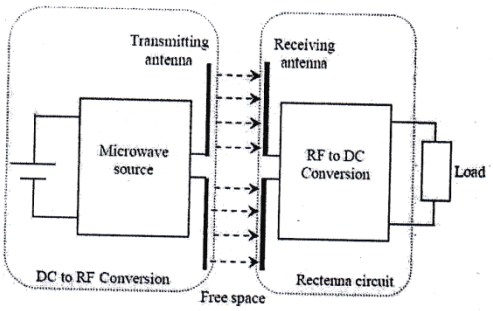


Fig.1 basic design of wireless power transmission

(Image courtesy form reference 8)

RELATED WORK:

As per the literature survey the newest technologies depend on inductive coupling methods to conduct power between transmitting and receiving coils [7]. The frequency at which the device

COMMITTEE

CHIEF PATRONS

Dr. S. Cletus Babu,
Chairman,
SCAD Group of Institutions, India.

Mr. C. Arun Babu,
Managing Director,
SCAD Group of Institutions, India.

Ms. C. Anandhi Babu,
HR Director,
SCAD Group of Institutions, India.

PATRONS

Mrs. J.J. Menandez,
Executive Director,
SCAD Group of Institutions.

Mr. A. Ignatious Xavier,
General Manager-Finance,
SCAD Group of Institutions.

Dr. K. Jeyakumar,
Professor & General Manager (Development),
SCAD Group of Institutions.

Mr. S. Krishna kumar,
Assistant General Manager,
SCAD Group of Institutions.

Prof.J.Monimoran,
Principal/AGM, SCAD Campus

Prof.S.Jeya Pandi,
Administrative Officer,
SCAD College of Engineering and Technology.

CONFERENCE CHAIR

Dr.P. Ebby Darney,
Principal,
SCAD College of Engineering and Technology, Tirunelveli,
TamilNadu, India.

CONFERENCE CO-CHAIR

Dr.R.Karthik Ganesh,
Associate Professor, Dept. of CSE,
SCAD College of Engineering and Technology.

SUBMISSION

Submit the paper through email to
icoei.conf@gmail.com

REGISTRATION DETAILS

Category		Registration Fee	
		IEEE Member	Non - IEEE Member
Indian Author	**Author** (Fee for 6 pages) For every extra page pay INR 500 Maximum number of pages: 8	INR 6000	INR 7000
	Listener	INR 3000	INR 4000
Foreign Author	**Author** (Fee for 6 pages) Maximum number of pages: 8	150 USD	200 USD
	Listener	100 USD	125 USD

CONTACT DETAILS

Dr. R. Karthik Ganesh,
Associate Professor, Dept. of CSE,
SCAD College of Engineering and Technology.
Email: icoei.conf@gmail.com
Contact: +91 9600368297

CONFERENCE URL:

http://icoei.com/2020/contact.html

Scopus®

IEEE

4TH INTERNATIONAL CONFERENCE ON TRENDS IN ELECTRONICS AND INFORMATICS

(ICOEI 2020)

CONFERENCE DATES: 16-18, APRIL 2020

ORGANIZED BY

SCAD COLLEGE OF ENGINEERING AND TECHNOLOGY
Cheranmahadevi, Tirunelveli,
Tamilnadu, India.

PUBLICATION:

Accepted and presented papers will be submitted for inclusion into IEEE Xplore.

SCAD COLLEGE OF ENGINEERING & TECHNOLOGY
Recognized by UGC under the section 2(f) & 12(B) of UGC Act, 1956 | Approved by AICTE & Affiliated to Anna University | ISO Certified Institution
Empowering Education... Global Leadership
Cheranmahadevi, Tirunelveli

ICOEI 2020

IEEE

CERTIFICATE OF PRESENTATION

This is to certify that

S Christo Jain

has successfully presented a paper entitled

Proposal of a cost-effective wireless Power Transfer system from Solar using Aerial Technology

in the ***4th International Conference on Trends in Electronics and Informatics (ICOEI 2020)*** *organised by SCAD College of Engineering and Technology, Tirunelveli, Tamil Nadu, India during 15-17, June 2020.*

SESSION CHAIR

ORGANIZING SECRETARY
Dr. I. Jeena Jacob

CONFERENCE CHAIR
Dr. P. Ebby Darney

IEEE XPLORE ISBN : 978-1-7281-5518-0

2020 4th International Conference on Trends in Electronics and Informatics (ICOEI 2020)

Tirunelveli, India
15 – 17 June 2020

Pages 1-539

IEEE

IEEE Catalog Number: CFP20J32-POD
ISBN: 978-1-7281-5519-7

Proposal of a cost-effective wireless Power Transfer system from Solar using Aerial Technology

S Christo Jain[1]
Research Scholar
Dept of Electronics and Communication
K.S. Institute of Technology
s.christojain@gmail.com

Dr.Manju V C[2]
Professor
Dept of Telecommunication
K S Institute of Technology
manju_tvm@yahoo.com

Abstract-The proposed system focus on reducing the complexity and power loss during transmission of electricity. Since we are using solar energy to harvest electricity we can avoid shedding down of power supply as well as we can reduce the complexity since no wire is required for transmission. Through this system we are focusing to supply electricity in remote areas where cable connection does not reach. This system is eco-friendly , cheap and portable. Our system uses sunlight to produce power and this shall be transfer to devices with the help of aerial. We can avoid breakage of electric lines and poles as well as transformer explosion.

Keywords : Solar, Aerial, wireless power transfer

I. INTRODUCTION

Solar panel electricity systems also known as photovoltaics (PV), pick up the sun's energy through photovoltaic cells [10]. These cells convert sunlight into power, which can be used to run household devices. In wire power supply pre planning is required to install wires for power supply; As we are using wireless power supply device, we do not require pre planning for installation as this device is flexible. In wide space areas long extension wires are used which make the rooms clumsy and disturbance in walk area may occur, these problems can be avoided in wireless power supply. The system is very simple and cheaper and is also portable. The system is easy to maintain and also comfortable. In modern world people do not like too much of wires hanging in the house; and using this device we can avoid usage of wires. Strong winds can break tree barks or entire trees on transformer causing them to fall on the ground ,Severe winds can even break electric lines and poles, bring down a considerable part of extent in the infrastructure that delivers power ,This problem is not seen in wireless power supply. Transformer explosions can also avoidusing Wireless power supply device.

Solar power is nothing but the heat outcome from the sunwhichisrenewedintoelectricalpower.Withasolar arrangement, you can make free power anywhere thesungleamseveninremotelocations[5].WPTorWET is transmission of electrical energy without using of anyphysicaldeviceamongtransmittersidetoreceiver side. This technology transmitter operated by electrical power from a power source which generates a time varying electromagnet, which transmitspoweracrossspacetoareceiverdevice,then itsuppliedtotheloadthroughpowerconvertercircuit. The skill of wireless power transmission can remove the use of batteries and wires .This will make an isolation between transmitter and receiver. This method save load from unwanted power and provide safety to the user. One of the difficulties in remaining power system is the victims taking place in the transmission and division of energy to the end users. The supply of the electricity happens through chords to the distribution lines. The key problem faced all through the power transmission is the victims that occur thru the transmission and distribution due to Power converter andcontrollers.

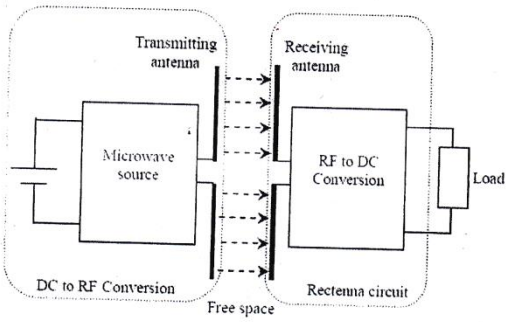


Fig.1 basic design of wireless power transmission
(Image courtesy form reference8)

We are using array of half wave Dipole aerial in the proposed system. A dipole is the simplest and most widelyusedclass of aerial. A dipole aerial commonly consists of two identical conductive elements such as metal wires orrods.The half wave dipole is the utmost widespread kindof the dipole aerial. Antenna extent is half in its signalwavelength. This will make suitable radiationpattern.

II. RELATED WORK:

As per the literature survey the newest technologies depend on inductive coupling methods to conduct power between transmitting and receiving coils [7]. The frequency at which the device transfers power between the transmitter and receiver is dependent on the size of the coils. The small transmitting and receiving coils able to transfer high frequency signal and also used Wireless Power Transfer using Radiative Technology. With Inductive coupling, the usage of Antenna for WPT is increasing currently. R.Marino, R.Mashiah, H.Matzner, E.Levine discovered an idea to use Fed Horn Antenna for transmitting power wirelessly [1]. Our system planning to use half wave dipole antenna for transmission and reception of power.Jae-Min Lee, designed horn aerial for high power microwave applications[4]. The authors Tae-Dong Yeo, DukSoo Kwon, Seung-Tae Khang and Jong-Won Yu, designed Maximum Efficiency Tracking Control Scheme for Closed Loop Wireless Power Charging System[6]. Wireless power transfer is one of the highest and excessive triumph of manhood has always been.Reaping Energy using renewable bases has been in the key concern of the research world in current years [2]. In the beginning American scientist, Nikola Tesla of the year 1856, designed a WPT using inductance[9],[11].Wireless mobile charger has been developed using inductive coupling.[3]; which is considering the base of our

A Survey on Machine Learning enabled SWARM robots for Autonomous and Precision Agriculture

Sampath Kumar.S, Research Scholar, KSIT, Bangalore, India
ShanthiPrasad.M.J, Professor, CITech. North Campus, Bangalore, India

Abstract:--
Machine learning has evolved with high performing computing algorithms along with Robotics and Artificial intelligence technologies. SWARM robotic system is a diligence of multi robot intelligence with collaborative communication approach. SWARM robots play a major role in precision agriculture. SWARM robots mainly focus on aspects like coordination, decentralized control and self organization. These technologies have created new opportunities in multidisciplinary agricultural domain. Integration of Machine learning principles with SWARM robotics will form a novel solution to make agricultural practice even more intelligent and accurate. In this paper, we present a comprehensive review of research related to adoption Machine learning principles in precision agriculture for various autonomous agricultural activities using SWARM robots.

Keywords:--
SWARM Robots, Precision Agriculture, Self Learning, Decision Tree, Random Forest, Knn Algorithm, Sowing, irrigation

ISBN: 978-93-89107-71-5

Organized by:
Cambridge Institute of Technology North Campus (CITNC), Bengaluru, Karnataka, India
and
Institute For Engineering Research and Publication (IFERP)

IEEE.org IEEE *Xplore* IEEE SA IEEE Spectrum More Sites Donate Cart Create Account Personal Sign In

Browse My Settings Help Access provided by: **K S Institute of Technology - Bengaluru** Sign Out

Access provided by: **K S Institute of Technology - Bengaluru** Sign Out

All ADVANCED SEARCH

Conferences > 2019 Global Conference for Ad...

Design & Modeling of Input Output Functionalities of FPGA based IO Block

Publisher: IEEE Cite This PDF

Aruna Rao B P ; Shanthi Prasad M .J **All Authors** •••

39 Full Text Views

Alerts

Manage Content Alerts

Add to Citation Alerts

Down
PDF

Abstract: As a part of my ongoing research towards Development of next generation High speed I/O&in continuation with the 2 technical survey papers already published by me I am bri... **View more**

▸ Metadata

Abstract:
As a part of my ongoing research towards Development of next generation High speed I/O&in continuation with the 2 technical survey papers already published by me I am bringing this research experiment paper covering - basic I/O concepts, functions, improvements, challenges found in the existing I/O, synchronization issues, open issues, case studies of Xilinx IO block. I have proposed a novel architecture to implement critical High speed I/O functions. I made designs for Digital modules, coded in Verilog & simulated in Xilinx ISE 14.5 to verify the functionality.

Published in: 2019 Global Conference for Advancement in Technology (GCAT)

Date of Conference: 18-20 October 2019

DOI: 10.1109/GCAT47503.2019.8978325

Date Added to IEEE *Xplore*: 03 February 2020

Publisher: IEEE

Conference Location: Bangalore, India

▼ ISBN Information:

Electronic ISBN:978-1-7281-3694-3
CD:978-1-7281-3692-9
USB ISBN:978-1-7281-3693-6
Print on Demand(PoD) ISBN:978-1-7281-3695-0

IEEE Bangalore Section

NAGARJUNA College of Engineering & Technology

GLOBAL CONFERENCE FOR ADVANCEMENT IN TECHNOLOGY
(Technically Co-Sponsered by IEEE Bangalore Section)

CERTIFICATE OF PRESENTATION

This Certificate is proudly presented to

Mr/Ms. ARUNA RAO B.P

From

KSIT, BANGALORE

for presenting paper entitled

"DESIGN AND MODELING OF INPUT OUTPUT FUNCTIONALITIES OF FPGA BASED IO BLOCK"

" GLOBAL CONFERENCE FOR ADVANCEMENT IN TECHNOLOGY "
Bangalore, India 18th - 20th October, 2019

Dr. Shantakumar B Patil
(General Chair)

Organised by : NAGARJUNA COLLEGE OF ENGINEERING AND TECHNOLOGY, BENGALURU

2019 Global Conference for Advancement in Technology (GCAT)

Design & modeling of Input Output Functionalities of FPGA based IO Block

Aruna Rao B P
Asst.Prof, ECE Dept
K.S Institute of Technology,
Bengaluru, India
Aruna.research2014@gmail.com

Dr. Shanthi Prasad. M .J
Professor, ECE Dept,
Cambridge Institute of Technology,
North Campus, Bengaluru.
prasadmjs@yahoo.com

***Abstract*-As a part of my ongoing researchtowardsDevelopment of next generation High speed I/O&in continuation with the 2 technical survey papers already published by me I am bringing this research experiment paper covering - basic I/O concepts, functions, improvements, challenges found in the existing I/O, synchronization issues, open issues, case studies of Xilinx IO block. I have proposed a novel architecture to implement critical High speed I/O functions.I made designs for Digital modules, coded in Verilog & simulated in Xilinx ISE 14.5 to verify the functionality.**

Keywords: Bidirectional I/O, Programmable select I/O, Boundary scan

I. INTRODUCTION

A. Basic I/O Concepts

Single-ended I/O has been the standard for years. In single-ended systems, one signal connection is made between the two ICs. This signal is compared to a specified voltage range (TTL CMOS [complementary metal oxide semiconductor]),[1] or a reference voltage (HSTL).

B. Basic Input/output System functions

- Communicate between chip and external world
- Drive large capacitance off chip
- Operate at compatible voltage levels
- Provide adequate bandwidth
- Limit slew rates to control di/dt noise
- Protect chip against electrostatic discharge
- Use small number of pins (low cost)

Input pad functions	Output pad Functions
• Level conversion • Higher or lower off-chip V • May need thick oxide gates • Noise filtering • Schmitt trigger • Hysteresis changes VIH, VIL • Protection against electrostatic discharge	• Drive large off-chip loads • With suitable rise/fall times • Requires chain of successively larger buffers • Guard rings to protect against latchup Noise below GND injects charge into substrate • Large nMOS output transistor

Bidirectional pads Functions	Analog pads functions
• Combine input and output pad • Need tri-state driver on output • Use enable signal to set direction • Optimized tri-state avoids huge series transistors	• Pass analog voltages directly in or out of chip • No buffering • Protection circuits must not distort voltages

C. High speed I/O –Open issues

- Level conversion
- High fan out
- Noise filtering
- Slew rate control
- Tristate

978-1-7281-3694-3/$31.00 ©2019 IEEE

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
IETE – 2020 Conference Proceedings

Design and Delay Analysis of Various 256-Bit Adders using Verilog

Rachana S
Department of ECE
K S Institute of Technology
Bangalore, India

Ritu Patil
Department of ECE
K S Institute of Technology

Sahana V
Department of ECE
K S Institute of Technology
Bangalore, India

Aruna Rao B P
Department of ECE
K S Institute of Technology
Bangalore, India

Abstract – **In this paper, several adders are being examined and compared in terms of delay of throughput. The objective of this paper is to design different architecture of adders and to observe the reliable output. Existing adder's performance will widely vary with respect to their area requirements and speed of execution. The proposed adder's architecture named Ripple carry adder, Carry look ahead adder, Carry skip adder, Carry save adder, Carry select adder, decomposes into blocks of carry generator, carry propagator and multiplexer. As Addition is the most important operation in data processing hence its speed has a significant impact on digital circuits. We have demonstrated the efficiency of the proposed architectures along with the design method in 256 bit operands.**

Keywords – Throughput, RTL schematic, Technological schematic, Simulation, Ripple carry adder, Operands, RCA (Ripple Carry Adder), CLA (Carry Look Ahead adder), CSkA (Carry Skip Adder), CSA (Carry Save Adder), CSlA (Carry Select Adder), ALU (Arithmetic Logic unit)

I. INTRODUCTION

Adders are called a digital circuit because they perform addition of numbers. It is a circuit that sums up the amplitude of 3 inputs that gives 2 outputs called sum and carry.They are being used in many processor architectures, ALU and computational units. Each adder creates a carry value which needs to be propagated via the circuit adders. Even though for many number of representations, adders can be constructed in the form of binary- coded decimal or excess-3, the most common adders operate on binary numbers.

RLA is a digital adder circuit, where in the carry out of every full adder will be the carry in of the next most significant full adder. It is so called because each carry bit receives rippled into the following next stage. CLA or fast adder is a type of digital circuit. It calculates one or more carry bits earlier than the sum, which reduces the wait or delay time. CSA is a form of virtual adder used in computer microarchitecture to locate the sum of 3 extra n-bit numbers in binary. CSlA is a way to enforce an adder, which may be a logic detail that finds out the sum of numbers. CSkA is a type of adder implementation that improves on delay of RCA when compared to other adders.

II. EXPRESSION OF ADDER

Sum = A^B^Cin
Carry = (A&B)|(B&Cin)|(Cin&A)
Carry generator = A&B
Carry propagator = A^B

Inputs			Outputs	
A	B	C – IN	Sum	C - Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 1: Truth Table

III. METHODOLOGY

A. Ripple Carry Adder

Basically, a full adder plays the addition operation on three inputs and produces the two outputs. Initially, it performs the addition on two inputs such as A and B along with the third input carry as C-IN. The two outputs produced are designated as S and C-OUT, where S is sum and C-OUT as carry-out. Full adder is designed with such a logic that it is capable of taking eight inputs at a time in order to create a byte-wide adder and the output carry is cascaded from one adder to another.

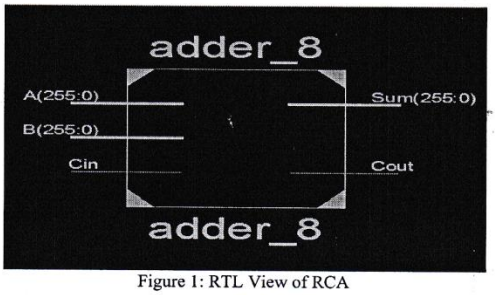
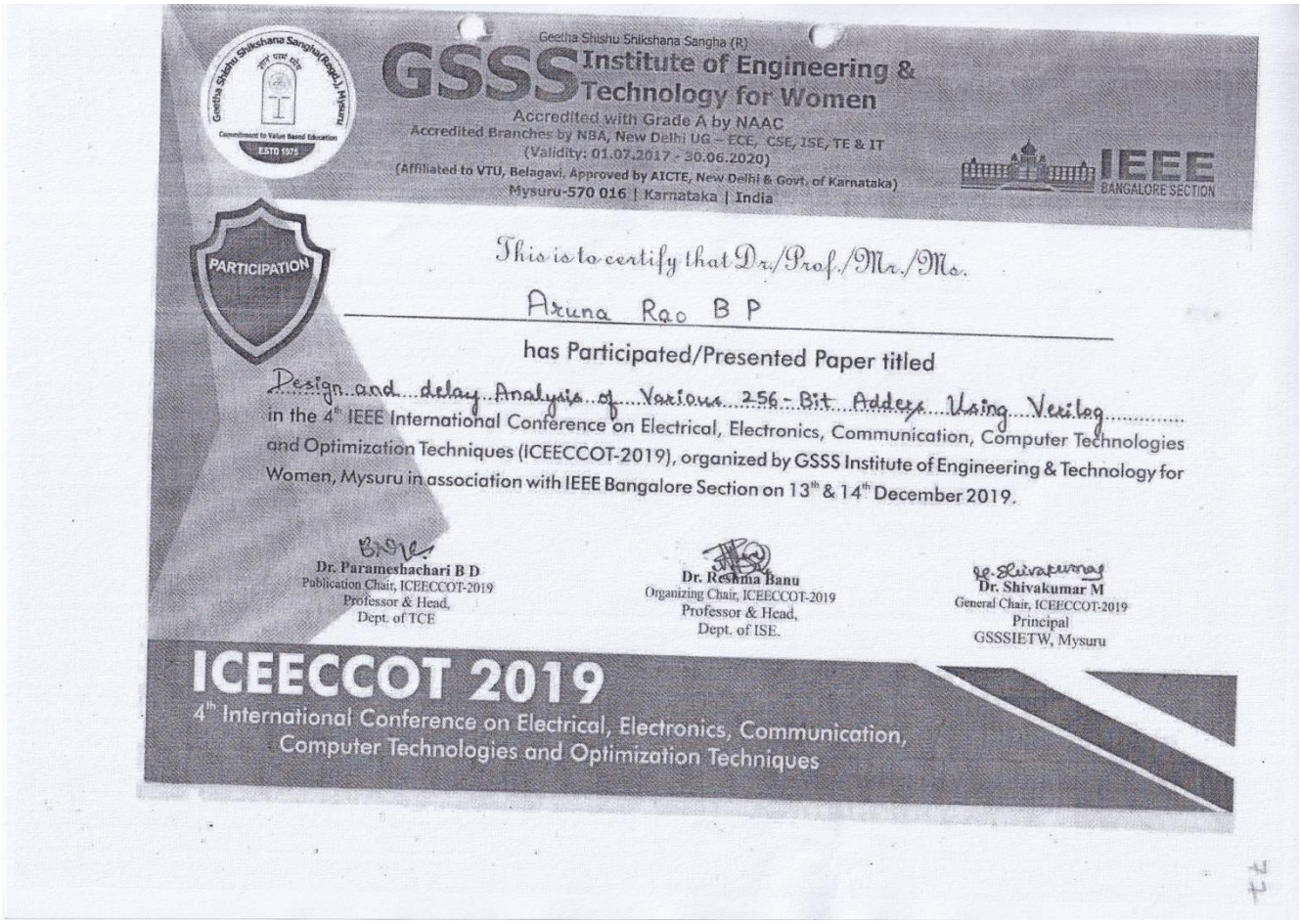


Figure 1: RTL View of RCA

Logical Expression for SUM:
= A' B' C-IN + A' B C-IN' + A B' C-IN' + A B C-IN
= C-IN (A' B' + A B) + C-IN' (A' B + A B')



Geetha Shishu Shikshana Sangha (R)

GSSS Institute of Engineering & Technology for Women

Accredited with Grade A by NAAC
Accredited Branches by NBA, New Delhi UG – ECE, CSE, ISE, TE & IT
(Validity: 01.07.2017 - 30.06.2020)
(Affiliated to VTU, Belagavi, Approved by AICTE, New Delhi & Govt. of Karnataka)
Mysuru-570 016 | Karnataka | India

IEEE BANGALORE SECTION

PARTICIPATION

This is to certify that Dr./Prof./Mr./Ms.

Aruna Rao B P

has Participated/Presented Paper titled

Design and delay Analysis of Various 256-Bit Adders Using Verilog

in the 4th IEEE International Conference on Electrical, Electronics, Communication, Computer Technologies and Optimization Techniques (ICEECCOT-2019), organized by GSSS Institute of Engineering & Technology for Women, Mysuru in association with IEEE Bangalore Section on 13th & 14th December 2019.

Dr. Parameshachari B D
Publication Chair, ICEECCOT-2019
Professor & Head,
Dept. of TCE

Dr. Reshma Banu
Organizing Chair, ICEECCOT-2019
Professor & Head,
Dept. of ISE.

Dr. Shivakumar M
General Chair, ICEECCOT-2019
Principal
GSSSIETW, Mysuru

ICEECCOT 2019

4th International Conference on Electrical, Electronics, Communication, Computer Technologies and Optimization Techniques

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
IETE – 2020 Conference Proceedings

Design and Implementation of 256*256 Booth Multiplier and its Applications

G S Surabhi
Department of Electronics and Communication,
K.S. Institute of Technology,
Bangalore

Bhavana. J
Department of Electronics and Communication,
K.S. Institute of Technology,
Bangalore

Madhu. S
Department of Electronics and Communication,
K.S. Institute of Technology,
Bangalore

ArunaRao. B. P
Department of Electronics and Communication,
K.S. Institute of Technology,
Bangalore

***Abstract*-This paper presents design of a booth multiplier which performs both signed and unsigned multiplication. This implementation describes in the form of RTL schematic. In the field of digital signal processing and graphics applications, multiplication is an important and is an application that demands a lot of computations. In this paper, we describe the implementation of 256-bit booth multiplier by comparing it with 64-bit and 128-bit booth multipliers. Booth algorithm employs both addition and subtraction and it also treats positive and negative operands uniformly. The proposed multiplier will be designed and verified using modalism with Verilog HDL, Xilinx is used for synthesis. This paper gives a complete idea of radix-64, radix-128, radix-256form booth algorithm.**

Keywords-Booth Multiplier, Xilinx, readix-256,radix-128, radix-64, multiplication.

I.INTRODUCTION

The multiplication of two binary inputs leads to manynumbers of gate count which occupies a large chip area on the digital system. The algorithm of booth multiplier furnishes a level to formulate a multiplier with greater effectiveness and speed. This algorithm is a better level of encoding.

The Booth multiplier makes use of addition and shifting algorithm. As compare to adder and subtractor multiplier are more complex. Multipliers play aimportant role in digital signal processing and other various applications. In this algorithm a partial product is generated by the multiplication of multiplicand with each bit of the multiplier.

A shift register is a very important digital building block. It has a large amount of applications. Registers are often used to store binary information appearing at the output. Shift registers are the logic types which are used for the storage and transfer of digital data. Multipliers are most commonly used in various electronic applications.

II. LITERATURE SURVEY

This paper briefly describes the method of implementing a digital multiplier called modified booth multiplier. From past one decade a number of efforts have been made to reduce dynamic power consumption in partial product generation and the power adder circuits about 40% of the research is on techniques for reducing partial products by changing the design of the modified booth multiplier.60% is on implementing low power adder circuits, error correction methods and circuit level power optimization techniques. A review from the earlier literature in this area is discussed in this report.

D.Govekar.al develop high speed modified both multipliers using hybrid adder. By employing modified booth multiplier design using hybrid adder shows better performance compare to conventional method of using carry look ahead adder.

Nagarjuna et.al has represented FIR Filter using the idea of multipliers with the reduction of bit size an elements source. FIR framework is applied using the enhanced edition unit multiplier. In proposed technique a booth multiplier is applied in this multiplier signed multiplication is an added advantage.

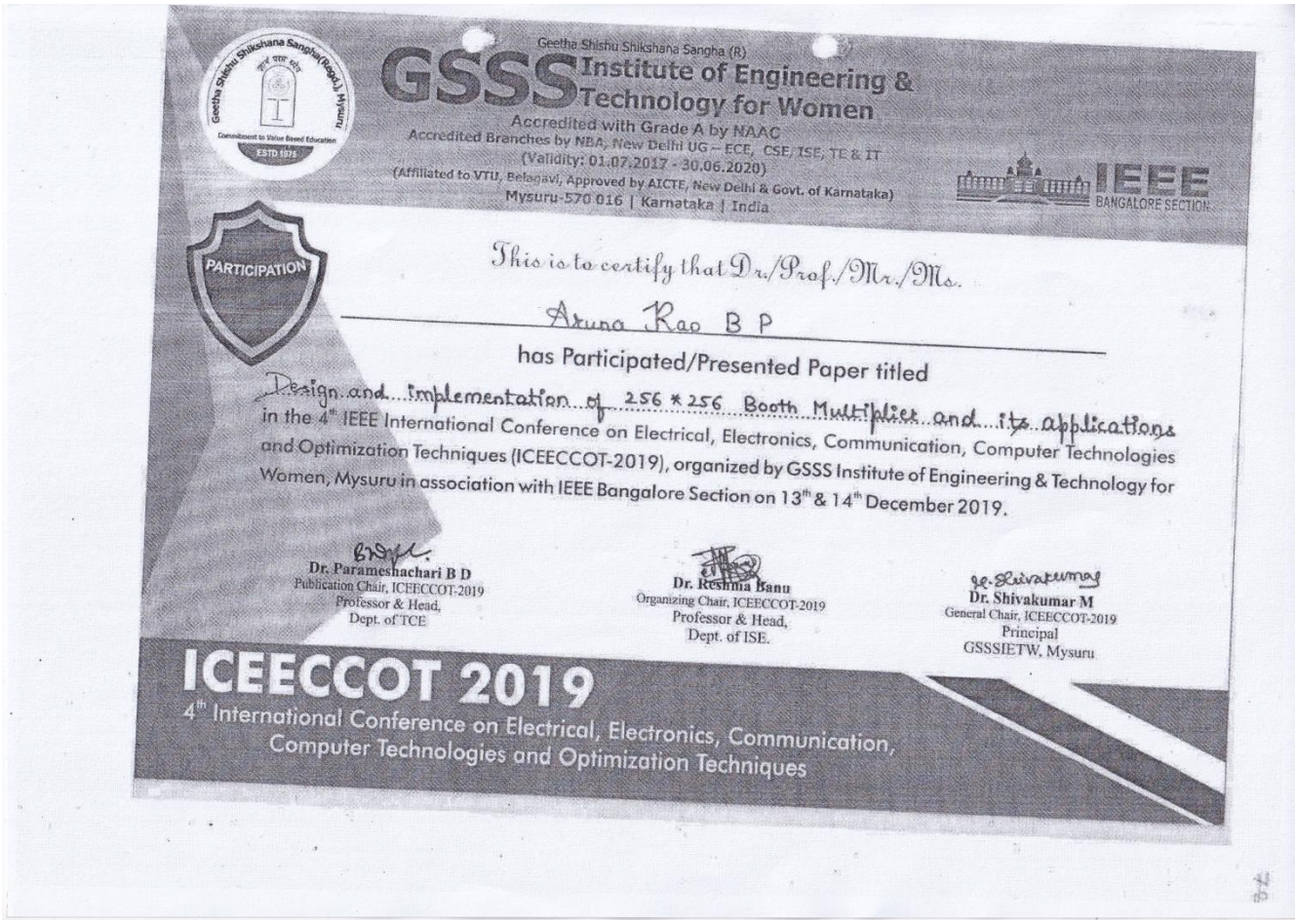
Honglan Jiang Fie has represented two signed 16*16-bit approximate radix-8 booth multipliers are designed using approximate recording adder with and without truncation of several less significant bits in the partial products. Multiplier are faster and more power efficient.

Prasanna Raj P Ravi has published a paper on analysis of multipliers for low power in, September 2009. In this paper they said that low power multipliers with high clock frequencies play an important role in today's digital signal processing.

Shwetha Khatri et.al, presents the FPGA implementation of a 64-bit fast multiplier using barrel shifter.in this research they have described the implementation of a 64-bit Vedic multiplier which is enhanced in terms of propogation delay. When it is compared with conventional multiplier like modified booth multiplier, Wallace tree multiplier, Braun multiplier, Vedic multiplication techniques for arithmetic operator. Synthesis report and static timing report used for the comparison of propogation delay. The design uses barrel shifter in base selection module and multiplier which achieves propogation delay of 6.78 Ins

III. ADVANTAGES

1. Booth multipliers are easily extensible.
2. These multipliers are easily pipelined.
3. Booth multiplier minimizes complexity.



Geetha Shishu Shikshana Sangha (R)

GSSS Institute of Engineering & Technology for Women

Accredited with Grade A by NAAC

Accredited Branches by NBA, New Delhi UG – ECE, CSE, ISE, TE & IT

(Validity: 01.07.2017 - 30.06.2020)

(Affiliated to VTU, Belagavi, Approved by AICTE, New Delhi & Govt. of Karnataka)

Mysuru-570 016 | Karnataka | India

IEEE BANGALORE SECTION

PARTICIPATION

This is to certify that Dr./Prof./Mr./Ms.

Aruna Rao B P

has Participated/Presented Paper titled

Design and implementation of 256 * 256 Booth Multiplier and its applications

in the 4th IEEE International Conference on Electrical, Electronics, Communication, Computer Technologies and Optimization Techniques (ICEECCOT-2019), organized by GSSS Institute of Engineering & Technology for Women, Mysuru in association with IEEE Bangalore Section on 13th & 14th December 2019.

Dr. Parameshachari B D
Publication Chair, ICEECCOT-2019
Professor & Head,
Dept. of TCE

Dr. Reshma Banu
Organizing Chair, ICEECCOT-2019
Professor & Head,
Dept. of ISE.

Dr. Shivakumar M
General Chair, ICEECCOT-2019
Principal
GSSSIETW, Mysuru

ICEECCOT 2019

4th International Conference on Electrical, Electronics, Communication, Computer Technologies and Optimization Techniques

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
IETE – 2020 Conference Proceedings

High Speed Multipliers and Complex Summers

Rahul R Nadig
Department of Electronics and Communication
K S Institute of technology,
Bangalore India

Pavan Prasad
Department of Electronics and communication
K S Institute of technology,
Bangalore India

Aruna Rao B P
Department of Electronics and Communication
K S Institute of technology,
Bangalore India

***Abstract*-Adders are basic digital circuits that perform binary addition. There are wide range of applications of adders depending upon the way they are implemented. Considering the fact that multiplication is successive addition, a multiplier is synthesised by multiplication of least significant bit (LSB) of multiplier with the multiplicand, binary addition of the product gives the result. Complex summers are designed by adding individual terms (real & imaginary) separately to give out the sum in terms of real and imaginary.**

Keywords- Adders, multiplier, summer, Xilinx tool

I. INTRODUCTION

Adders are of two kinds. Half adders and full adders, half adders are used when there are two inputs are of single bit. Full adders are used when there are three inputs of single bit. The truth table of half adder is shown in table1.

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Table 1: Half adder truth table

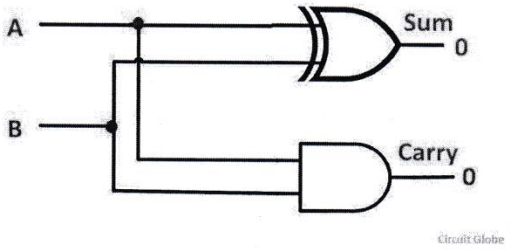


Figure 1: Half Adder circuit

The truth table of full adder is shown in table2.

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 2: Full adder truth table

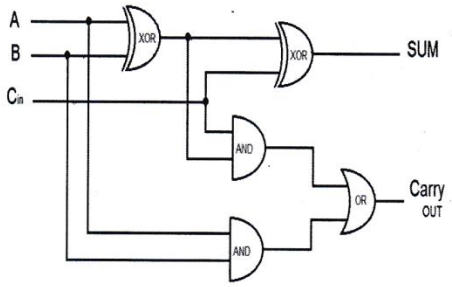


Figure 2: Full adder circuit

When the number of inputs increases the speed of calculation decreases. To improve the speed Carry Look Ahead adders are considered wherein the amount of time required to calculate the carry bit is less. A carry look adder uses the concept of generator and propagator. Its advantage is wide variety of applications (multiplier and complex summer) that can be realised and implemented on a suitable hardware. The major disadvantage is as the number of variables increases the complexity of the circuit increases. The circuit is costlier as it involves a greater number of hardware. Multiplication is considered as successive addition, based on this logic a multiplier is designed using a carry look ahead adder.

A. Carry look ahead adder

A carry look ahead adder circuit consists of full adders in cascade and carry generation circuit. Each full adder generates a sum, generator and propagator expression simultaneously without a delay. The generator and propagator of each full adder is taken for the calculation the carry bit. A generator and propagator are given by,

Consider two inputs A, B of size 1 bit. A generator is given by G (A, B) =A&B.

A propagator is given by P (A, B) =A^B.

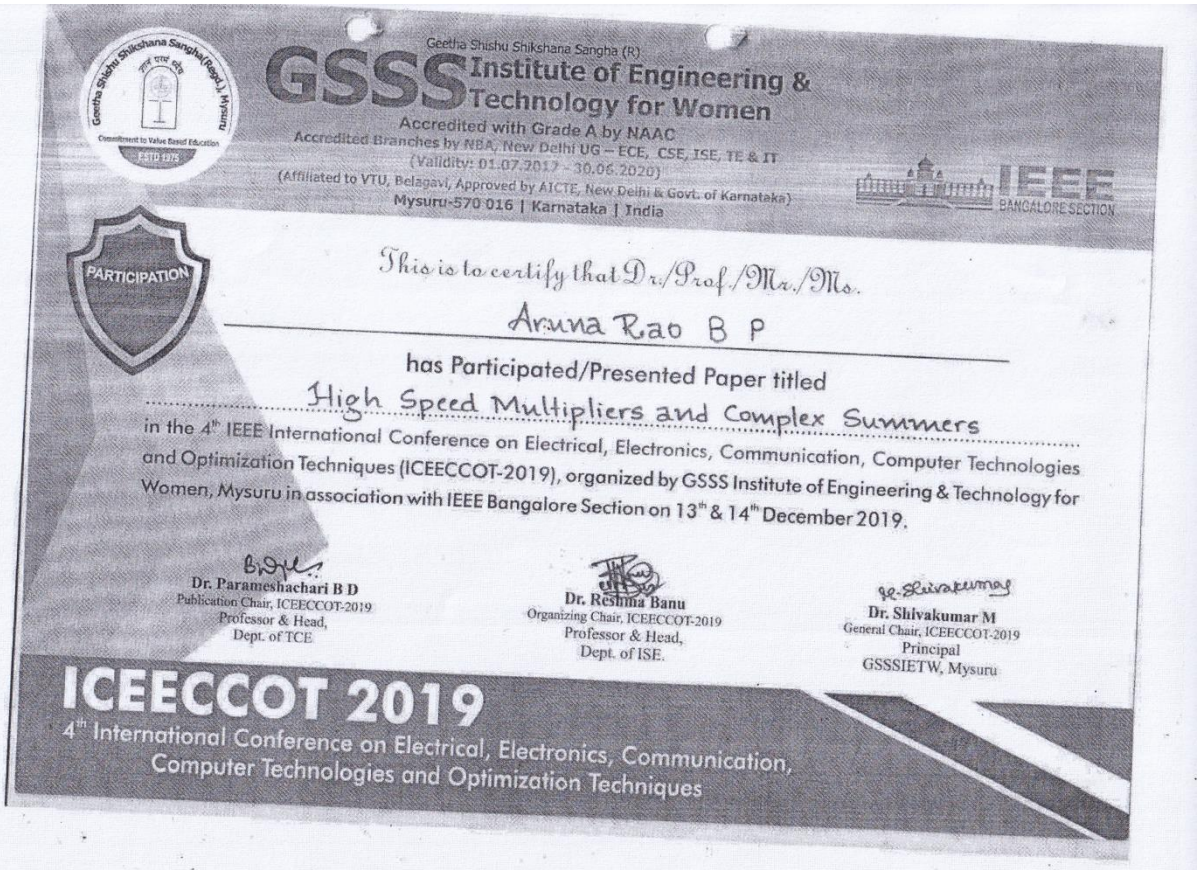
These two equations are used for the calculation of the summer) that can be realised and implemented on a carry bit given by the formula -

$C_{i+1} = G_i + (P_i * C_i)$.

Consider i=0 then, $C_1=G_0+(P_0*C_0)$

i=1 then, $C_2=G_1+(P_1*C_1)$

i=2 then, $C_3=G_2+(P_2*C_2)$



Geetha Shishu Shikshana Sangha (R)

GSSS Institute of Engineering & Technology for Women

Accredited with Grade A by NAAC

Accredited Branches by NBA, New Delhi UG – ECE, CSE, ISE, TE & IT

(Validity: 01.07.2017 - 30.06.2020)

(Affiliated to VTU, Belagavi, Approved by AICTE, New Delhi & Govt. of Karnataka)

Mysuru-570 016 | Karnataka | India

IEEE BANGALORE SECTION

PARTICIPATION

This is to certify that Dr./Prof./Mr./Ms.

Aruna Rao B P

has Participated/Presented Paper titled

High Speed Multipliers and Complex Summers

in the 4th IEEE International Conference on Electrical, Electronics, Communication, Computer Technologies and Optimization Techniques (ICEECCOT-2019), organized by GSSS Institute of Engineering & Technology for Women, Mysuru in association with IEEE Bangalore Section on 13th & 14th December 2019.

Dr. Parameshachari B D
Publication Chair, ICEECCOT-2019
Professor & Head,
Dept. of TCE

Dr. Reshma Banu
Organizing Chair, ICEECCOT-2019
Professor & Head,
Dept. of ISE.

Dr. Shivakumar M
General Chair, ICEECCOT-2019
Principal
GSSSIETW, Mysuru

ICEECCOT 2019

4th International Conference on Electrical, Electronics, Communication, Computer Technologies and Optimization Techniques

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
IETE – 2020 Conference Proceedings

Design and Implementation of Reversible Combinational Circuits by Creating Libraries of Basic Gates using Verilog HDL

M.Sirisha
Department of Electronics and Communication Engineering,
KS Institute of Technology,
Bangalore, India

Krithika.P
Department of Electronics and Communication Engineering,
KS Institute of Technology,
Bangalore, India

Anitha.R
Department of Electronics and Communication Engineering,
KS Institute of Technology,
Bangalore, India

Aruna Rao.B.P
Department Electronics and Communication Engineering,
KS Institute of Technology,
Bangalore, India

***Abstract*-This paper signifies the research work on design of reversible gates and various applications of it using Verilog HDL and VHDL with Xilinx ISE version 13.1, spartan 6 FPGA. Reversible gates have the facility to generate unique output vector from each input vector and vice-versa. Irreversible gates are the circuits which have an information loss. Losing information in a circuit causes losing power. So reversible gates have a better advantage when compared to irreversible gates. Using Verilog and VHDL we are creating a library of reversible gates such as AND, OR, CNOT, NAND, NOR, XOR. Using this library, we are implementing applications such as full adder, decoder (2:4),decoder (3:8),multiplexer, fullsubtractor, comparator.**

Keywords- Reversible logic, Irreversible logic, Xilinx, Spartan 6 FPGA, Library of basic gates, Implementation of digital circuits.

I. INTRODUCTION:

Computers today terribly waste energy and storage capacity. They throw away millions of bitsevery second. These are based on irreversible logic devices, which have been recognized as being fundamentally energy inefficient for several decades.So reversible gates are the best remedies.Reversible gates are the circuits in which losses are minimized. In these circuits number of inputs will be equal to the number of outputs and there is one to one mapping between vectors of inputs and outputs. Fredkin gate, Toffoli gate, interaction gate, and switch gate are typical ones.

Full adder- Adder is a digital circuit which adds n number of input bits with carry.Adder circuits are not only used in ALUs, but also used in various processors to calculate various increment or decrement operations, addresses, etc.

Multiplexer-Multiplexer is a device which has many inputs and only one output. It selects one of several analog or digital input signals and forwards the selected inputs into a single line.

Decoder-a binary decoder is a combinational logic circuit which converts binary information from n coded inputs to a maximum of 2^n unique output. The decoders are used in analog to digital conversion in analog decoders.

Fullsubtractor- A full subtractor is a digital combinational circuit that performs subtraction n input bits, taking borrow into consideration. They are used for mathematical calculation, electronic calculators and in digital devices.

Comparator-Comparator is an electronic combinational circuit that compares n input bits and it has 3 outputs namely lesser than, greater than and equal to. They are used in devices such as ADC, Oscillators, traffic lights, etc.

Reversible computing may have applications in computer security and transaction processing, but the main long-term benefit will be felt very well in those areas which require high energy efficiency, speed and performance.

- **Needand for reversible gates over irreversible gates:**

In recent times researchers have investigated various reversible logic gate and their all-feasible implementations.

Process improvements are eventually a dead end

- Energy usage will become prohibitive
- Heat dissipation will become more problematic

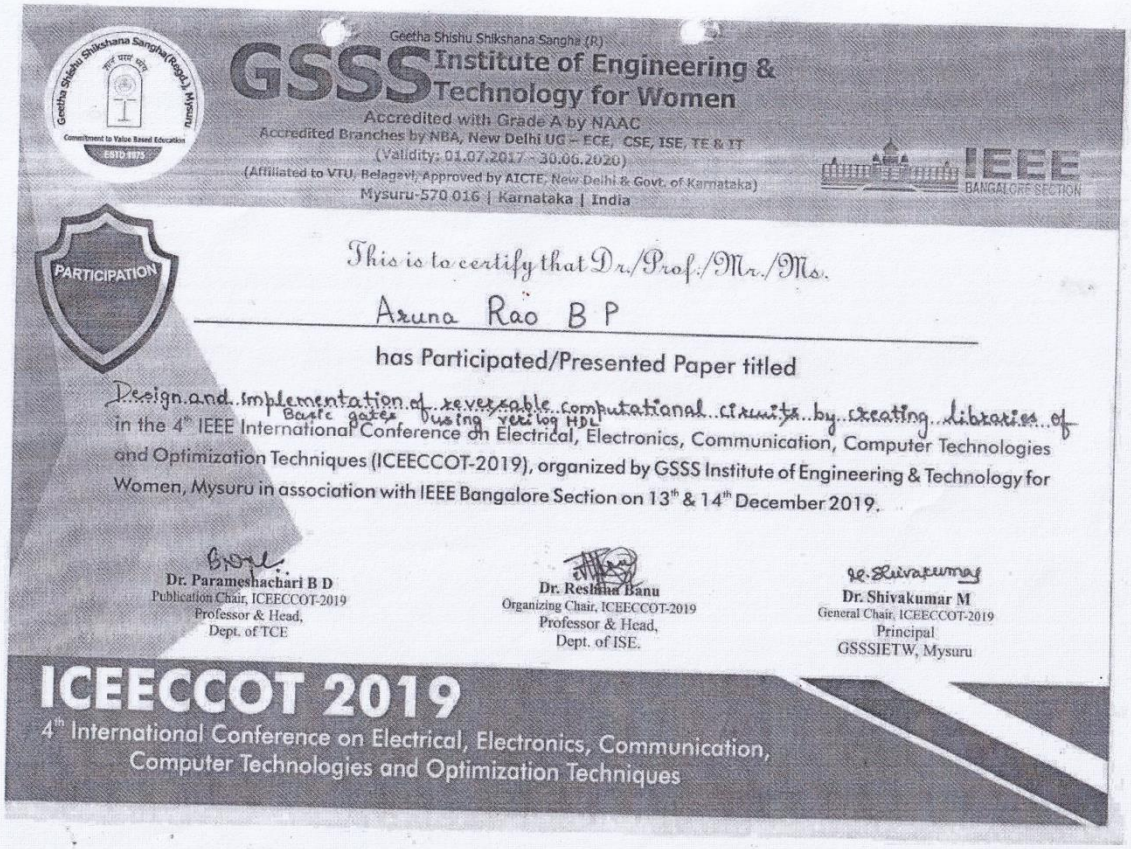
Classical computer dissipates a lot of energy

- Bulk electron processes

Many electrons used to do a single logical operation

II.PROCEDURE AND METHODOLOGY:

We are implementing applications like full adder, and multiplexer using XILINX ISE version 13.1 and spartan 6 FPGA. Xilinx ISE is a software tool produced by Xilinx for synthesis and analysis of HDL designs. This tool enables the developer to synthesise their designs, perform time analysis, examine RTL diagrams, design reactions to different stimuli, and configure the target device with the programmer. Spartan 6 FGPA is a hardware kit which is used for implementation of the developer designs. This kit is easy to use and implement any complex circuit using VHDL and Verilog HDL. FPGA -



Geetha Shishu Shikshana Sangha (R)

GSSS Institute of Engineering & Technology for Women

Accredited with Grade A by NAAC
Accredited Branches by NBA, New Delhi UG – ECE, CSE, ISE, TE & IT
(Validity: 01.07.2017 - 30.06.2020)
(Affiliated to VTU, Belagavi, Approved by AICTE, New Delhi & Govt. of Karnataka)
Mysuru-570 016 | Karnataka | India

IEEE BANGALORE SECTION

PARTICIPATION

This is to certify that Dr./Prof./Mr./Ms.

Aruna Rao B P

has Participated/Presented Paper titled

Design and implementation of reversable computational circuits by creating libraries of Basic gates using verilog HDL

in the 4th IEEE International Conference on Electrical, Electronics, Communication, Computer Technologies and Optimization Techniques (ICEECCOT-2019), organized by GSSS Institute of Engineering & Technology for Women, Mysuru in association with IEEE Bangalore Section on 13th & 14th December 2019.

Dr. Parameshachari B D
Publication Chair, ICEECCOT-2019
Professor & Head,
Dept. of TCE

Dr. Reshma Banu
Organizing Chair, ICEECCOT-2019
Professor & Head,
Dept. of ISE.

Dr. Shivakumar M
General Chair, ICEECCOT-2019
Principal
GSSSIETW, Mysuru

ICEECCOT 2019

4th International Conference on Electrical, Electronics, Communication, Computer Technologies and Optimization Techniques

Local Organizing Committee

Prof. C. Periasamy
Prof. R. Udayakumar
Prof. M. V. N. Sankaram
Dr. Shashank Khurana
Dr. Naveen Shrivastava
Dr. Snehaunshu Chowdhury
Dr. Gulshan Kumar

Key Dates

Abstract Submission	**30th July 2019**
Abstract Acceptance	**15th August 2019**
Manuscript Submission	**15th September 2019**
Manuscript Acceptance	**10th October 2019**
Early Bird Registration	**15th October 2019**
Registration Deadline	**10th November 2019**

Registration Fees

The registration fees for participants are

Participant Profile	Early Bird (15 Sep - 15 Oct)	Regular (16 Oct -10 Nov)
Delegates from Academic (Faculties, Post-Docs, R&D)	250 USD (920 AED)	300 USD (1100 AED)
Delegates from Industries	300 USD (1100 AED)	350 USD (1285 AED)
Student Delegate (Ph.D, M.Tech & B.Tech)	200 USD (735 AED)	250 USD (920 AED)

Registration fees include Publication charges, Registration kit, Lunch during conference days, Dhow Cruise and Desert Safari.
The mode of payment of registration fees will be provided in the website.(***www.immt2019.com***)

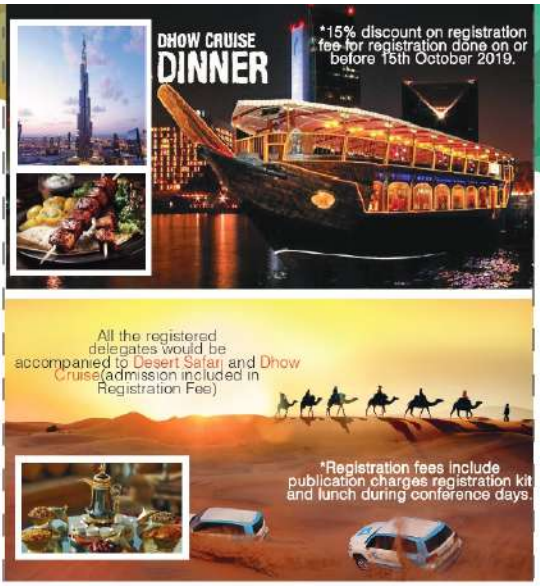
Publication

Peer reviewed and accepted papers will be published in *Scopus Indexed Elsevier Publication.*

ELSEVIER

Materials Today: Proceedings.

Previous Edition of the Conference IMMT 2017 was published in IOP Conference Series (*https://iop-science.iop.org/issue/1757-899X/346/1*)



Accommodation

Please check the conference website for accommodation options near venue. Single Hostel Rooms will be provided on request basis at nominal rates

For Futher Details

Dr. Vincent Shantha Kumar
Email id: vincent@dubai.bits-pilani.ac.in
Tel: +971 55 829 9787

Dr. Priyank Upadhyaya
Email id: priyank@dubai.bits-pilani.ac.in
Tel: +971 56 212 2713

DUBAI

2nd International Conference on Recent Advances in Materials & Manufacturing Technologies

IMMT 2019

Call for Abstracts & Papers

BITS Pilani
Dubai Campus

November 20-22, 2019

ELSEVIER

Organized by
Department of Mechanical Engineering
BITS Pilani Dubai Campus
Academic City
P.O.Box No. 345055
Dubai, U.A.E

immt2019@dubai.bits-pilani.ac.in

www.immt2019.com

ScienceDirect

Journals & Books

Access through your institution

Purchase PDF

materialstoday: PROCEEDINGS

Volume 28, Part 2, 2020, Pages 504-509

Processing and evaluation of Al/B_4C particulate MMC's: Tensile strength and wear properties under different elevated temperature test condition

Rajesh Gangadi Lakshmikantha, Virupaxi Auradi

Abstract

In the present investigation, preheated K_2TiF_6 flux were blended with B_4C particle (an average size of 33μm) at 0.2 ratios and were incorporated into molten Al at 750 °C through conventional stir casting. Microstructural studies of as cast 6xxx alloy and composite were done using SEM/EDS/XRD. A fairly uniform distribution of B_4C particles were observed throughout the matrix with few agglomeration at certain places. Ultimate tensile strength and wear behaviour of the prepared composite were tested using computer assisted UTM and Pin-On-Disk apparatus under elevated temperature (100 °C and 200 °C) respectively. The results shows that strength of composite decreases under the influence of temperature at all testing parameters. It is believed that material had undergone severe plastic deformation before the initiation of necking and mild brittle to severe ductile transition has occurred leading to catastrophic failure at high temperature and is evident from the fractography studies. The formation of tribo-coat or layer at the Pin sample and steel disc interface restricted the direct contact with each other. Further, the addition level of test temperature and developed frictional heat encourages Al atoms to diffuse faster at the slip plane resulting in severe wear from the material surface. Small narrow abrasive lines, particle de-bonding, softened tribolayer along with few wear debris adhered to worn surface (due to micro ploughing and oxidation) were observed on the surface of composite at all conditions under 200 °C test temperatures. Presence of "O" and "Fe" peak in the EDS pattern (on worn surface) confirms the existence of oxidation layer and micro ploughing on steel disc at higher test temperature.

Part of special issue

2nd International Conference on Recent Advances in Materials & Manufacturing Technologies

Other articles from this issue

Thermal and mechanical simulations of the lattice structures in the conformal cooling...

Effect of TiN addition on corrosion behavior of spark plasma sintered 304L austenitic...

Combined global-local monitoring of hydrating concrete using embedded smar...

View more articles

Recommended articles

Soldering aluminium to copper with the use of interlayers deposited by cold spraying

Strong crack blunting by shear-coupled migration of grain boundaries in...

Tensile properties of reactive stir-mixed and squeeze cast Al/CuO-based metal matri...